

C340

C340 INTEL H61 COUGAR POINT EVT Schematics

PCB Version : XXXXXXXXXXXXXXX

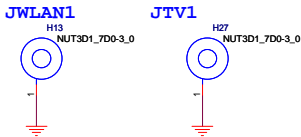
CONTENTS	SHEET
01 TABLE OF CONTENTS	1
02 SYSTEM BLOCK DIAGRAM	2
03 CLK/SMBUS/RESET MAP	3
04 CPU FM2 (1/4)	4
05 CPU FM2 (2/4)	5
06 CPU FM2 (3/4)	6
07 DDR3 SODIMM5.2	7
08 DDR3 SODIMM9.2	8
09 TRANSLATE ANX3110	9
10 MXM 3.0 TYPE-A	10
11 FCH UMI/PCIE/CLK/LPC (1/5)	11
12 FCH USB/AUDIO/GPIO/KB (2/5)	12
13 FCH SATA/SPI/VGA (3/5)	13
14 FCH STRAP PIN (4/5)	14
15 FCH POWER (5/5)	15
16 Audio Codec 92HD91/SSM2306	16
17 Audio DRV604/D-MIC	17
18 GIGA LAN RTL8111F/LED	18
19 CR/HDD/ODD/WEBCAM	19
20 MINI PCIe x 3/FAN	20
21 USB3.0/USB2.0 CONN/CHARGER	21
22 CIR/SCALAR/USB HUB/TOUCH	22
23 EC IT8519E	23
24 DEBUG CIRCUIT	24
25 SYSTEM +3V/+5V	25
26 +VDDIO_MEM/MEM_VTT/DC-IN	26
27 +1.1V/+1.2V	27
28 +12V/+2.5V/+1.1V	28
29 ISL6277	29
30 ISL6277/MOS	30
31 POWER SEQUENCE	31
32 HISTORY	32

PORT	NET NAME	FUNCTION
SATA_TX0P/N	SATA_TX0P/N	SATA HDD
SATA_RX0P/N	SATA_RX0P/N	
SATA_TX1P/N	SATA_TX1P/N	SATA ODD
SATA_RX1P/N	SATA_RX1P/N	
SATA_TX2P/N	SATA_TX2P/N	mSATA
SATA_RX2P/N	SATA_RX2P/N	

	PARTS	DIP/SMT	Frequence	PPM	CL
1	X1	SMT	25MHz	±20	10pF/10pF
2	X2	SMT	32.768KHz	±20	7pF/7pF
3	X3	SMT	25MHz	±20	10pF/10pF

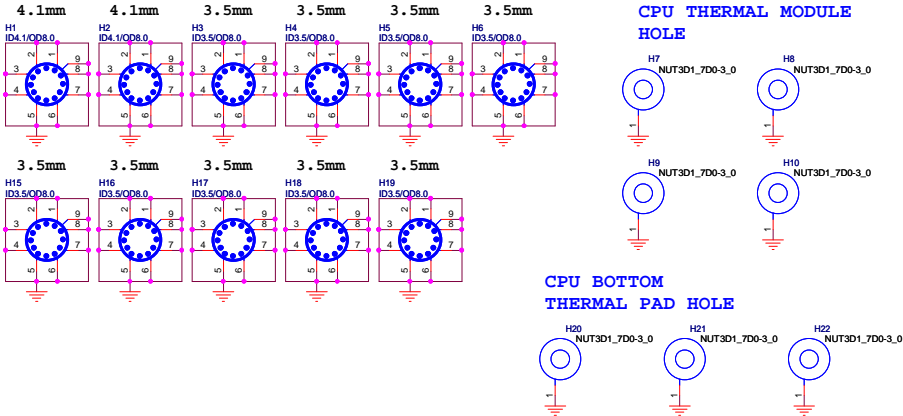
PORT	NET NAME	FUNCTION
USB_HSD0P/N	USB0_DEBUGP/N	SIDE IO
USB_HSD1P/N	USB1P/N	SIDE IO
USB_HSD2P/N	USB2P/N	REAR IO
USB_HSD3P/N	USB3P/N	REAR IO
USB_HSD4P/N	USB4P/N	REAR IO
USB_HSD5P/N	USB5P/N	REAR IO
USB_HSD6P/N	USB6_WLAN_P/N	WLAN CARD
USB_HSD7P/N	USB7_TV_P/N	TV CARD
USB_HSD8P/N	USB8_DONGLE_P/N	DONGLE
USB_HSD9P/N	USB9_HUB_P/N	HUB IC

PORT	NET NAME	FUNCTION
GPP_TX0P/N	PCIE_CR_TXP/N	CARD READER
GPP_RX0P/N	PCIE_CR_RXP/N	
GPP_TX1P/N	PCIE_TV_TXP/N	TV CARD MODULE
GPP_RX1P/N	PCIE_TV_RXP/N	
GPP_TX2P/N	PCIE_LAN_TXP/N	GIGA LAN
GPP_RX2P/N	PCIE_LAN_RXP/N	
GPP_TX3P/N	PCIE_WLAN_TXP/N	WLAN CARD MODULE
GPP_RX3P/N	PCIE_WLAN_RXP/N	
P_GFX_TX0~15P/N	GFX_APU_TXP/N 0~15	MXM
P_GFX_RX0~15P/N	GFX_APU_RXP/N 0~15	



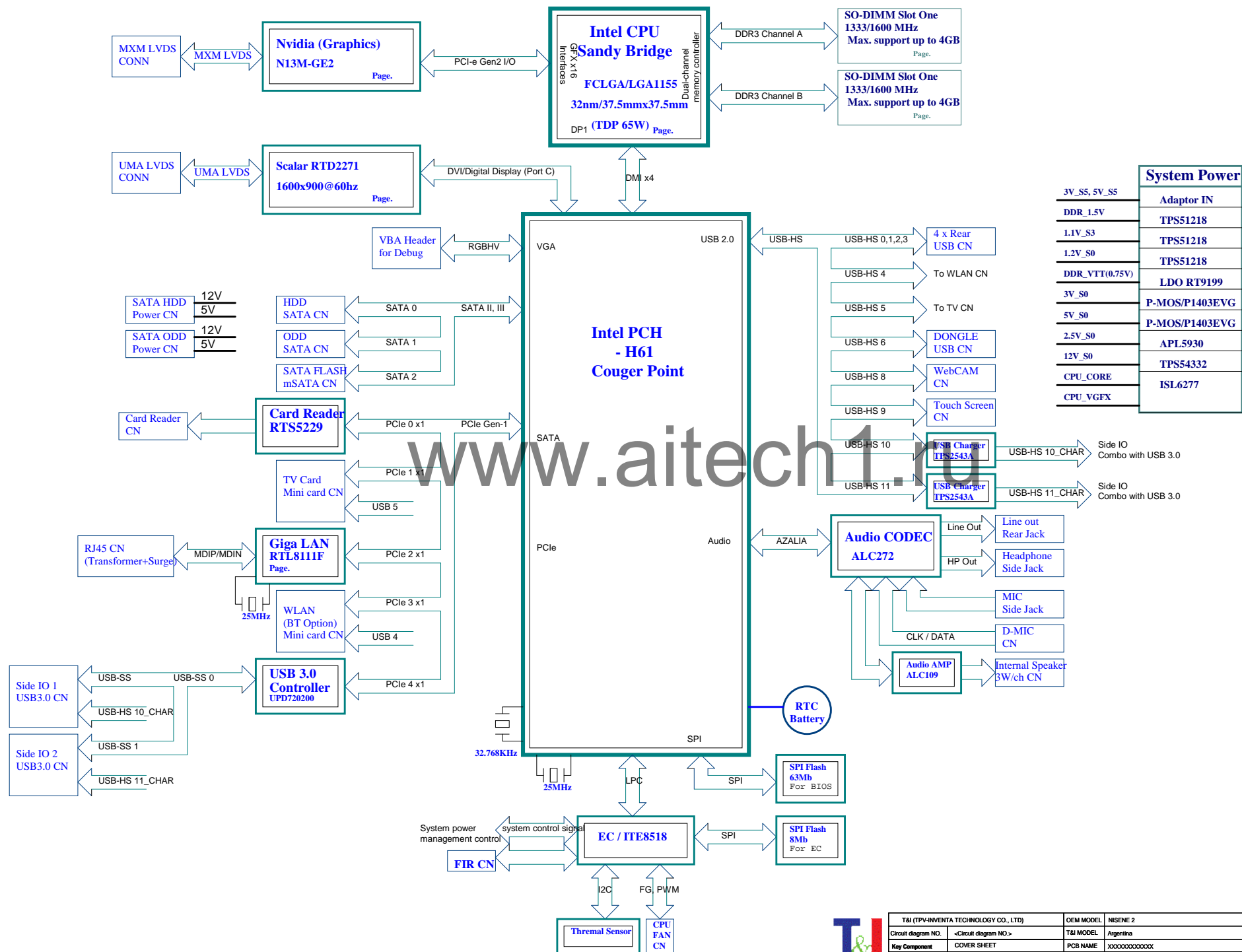
POWER STATES

STATE	VOTAGE	S0	S3	S5	G3	REMARK
SIGNAL						
FCH_SLP_S3#	-	HIGH	LOW	LOW	LOW	
FCH_SLP_S5#	-	HIGH	HIGH	LOW	LOW	
S5_PWR_ON	-	HIGH	HIGH	HIGH	LOW	S5_PWR_ON
+VBAT_IN	+3.3V	0	0	0	0	COIN BATTERY
+VIN	+19V	0	0	0	X	DC-IN
+3V_LDO/+5V_LDO	+3.3V/+5V	0	0	0	X	
+3V_S5	+3.3V	0	0	0	X	
+5V_S5	+5V	0	0	0	X	
+5V_S3	+5V	0	0	X	X	
+3V_S3	+3.3V	0	0	X	X	
+1.1V_S3	+1.1V	0	0	X	X	
+1.5V_S3	+1.5V	0	0	X	X	
+MEM_VTT	+0.75V	0	X	X	X	
+3V_S0/+5V_S0	+3.3V/+5V	0	X	X	X	
+12V_S0	+12V	0	X	X	X	
+1.8V_S0	+1.8V	0	X	X	X	
+1.5V_S0	+1.5V	0	X	X	X	
+1.05V_S0	+1.05V	0	X	X	X	
+CPU_VCCIO	+1.0V	0	X	X	X	
+0.85V_S0	+0.85V	0	X	X	X	
+CPU_AXG	SVC/SVD	0	X	X	X	
+CPU_VCC	SVC/SVD	0	X	X	X	



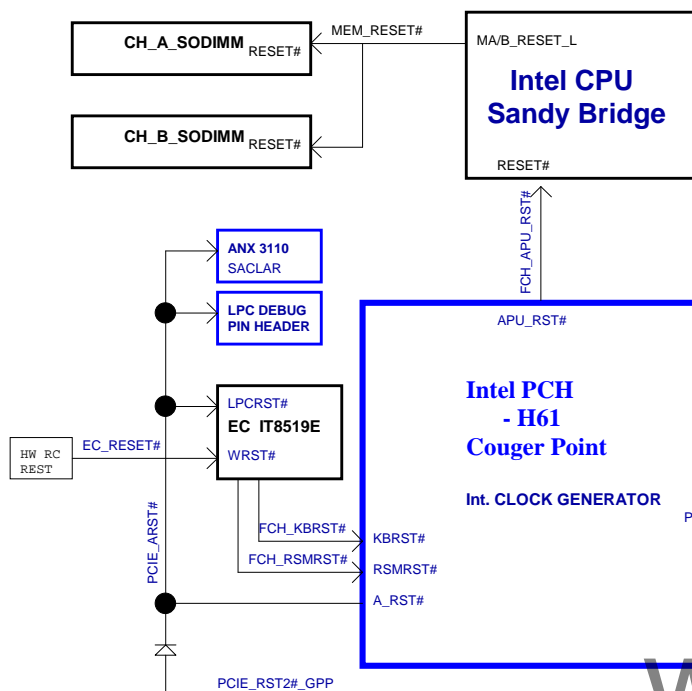
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark
Date	Thursday, December 22, 2011	Sheet	1 of 49	<remark>

# HP Nisene2 - Intel Snady Bridge

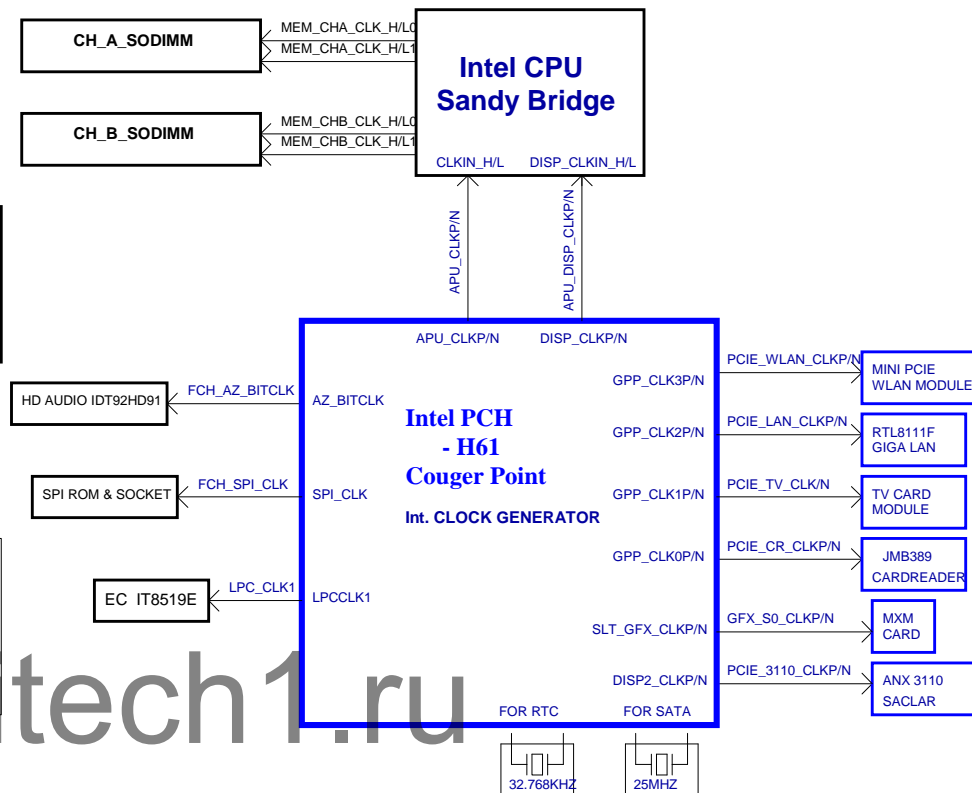


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev	RDA
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark	<remark>
Date	Thursday, December 22, 2011	Sheet	2 of 49		

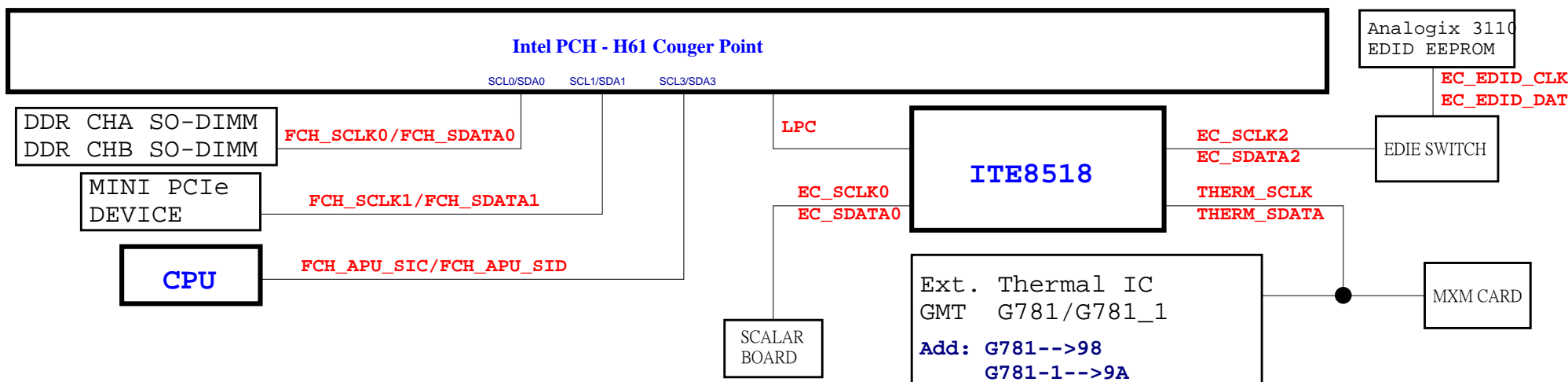
## RESET Block Diagram



## INTERNAL CLOCK MODE

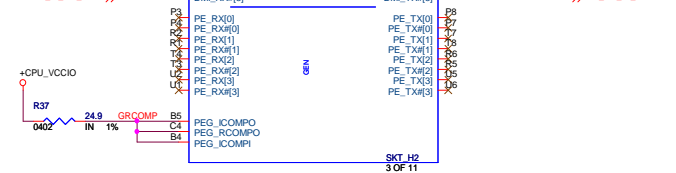
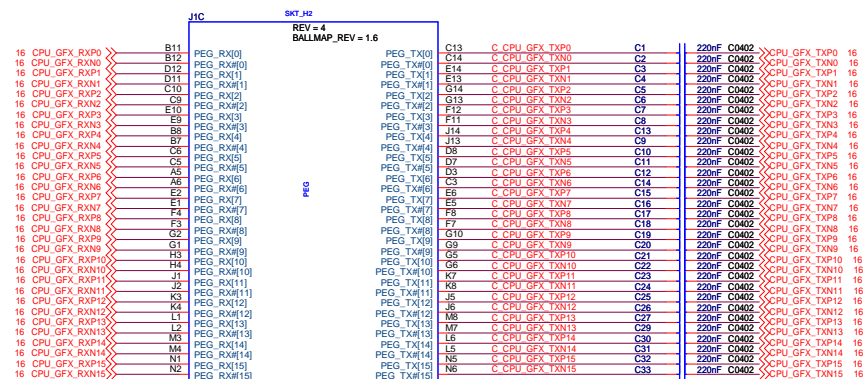


## SM Bus MAP



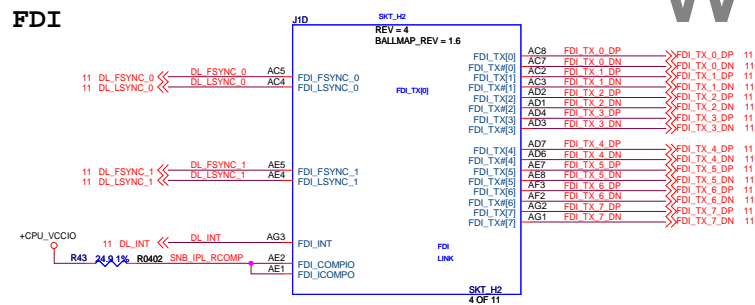
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark
Date	Thursday, December 22, 2011	Sheet	3 of 49	<remark>

## PCIEX16 & DMI

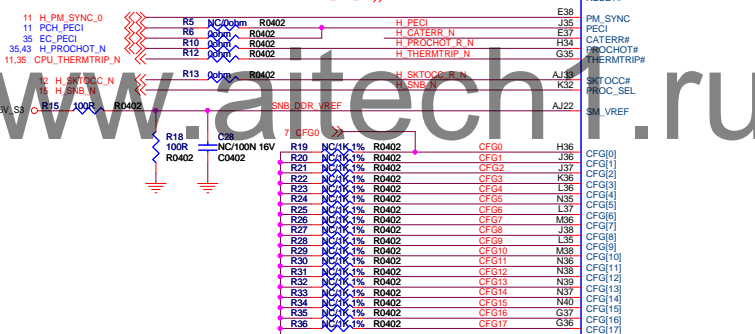
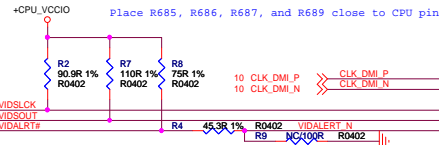
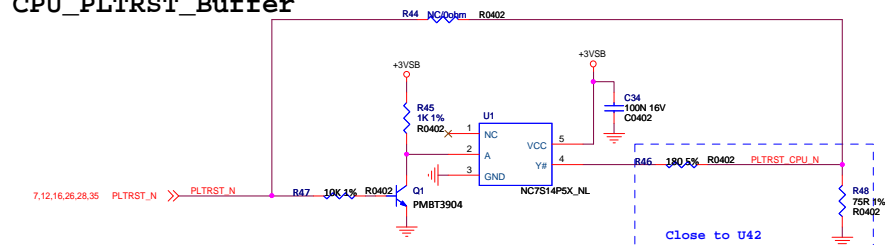


Note:

- (1).SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4 MIL TRACE TO R81
- (2).ROUTE B5 TO R81 AS A SEPERATE 12 MIL TRACE
- (3).PCIE X4 LANES ARE NOT SUPPORTED ON DESKTOP CPU SKUS

CPU PLTRST Buffer<sup>1</sup>

If PLT\_RST driver current enough. need to use buffer

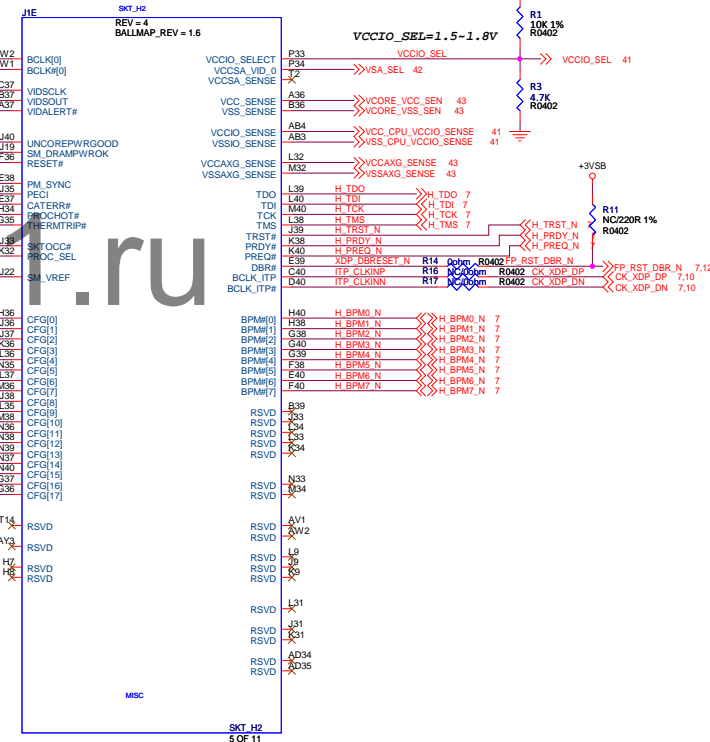


Below configuration is defined on CRB page 14

```
CFG2-->H-->NORM-->L-->REVERSE
CFG5-->SEL(0)-->H
CFG6-->SEL(1)-->H
1X16

CFG5-->SEL(0)-->L
CFG6-->SEL(1)-->H
2X8

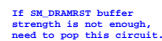
CFG5-->SEL(0)-->L
CFG6-->SEL(1)-->L
X8,X4,X2,X1
```

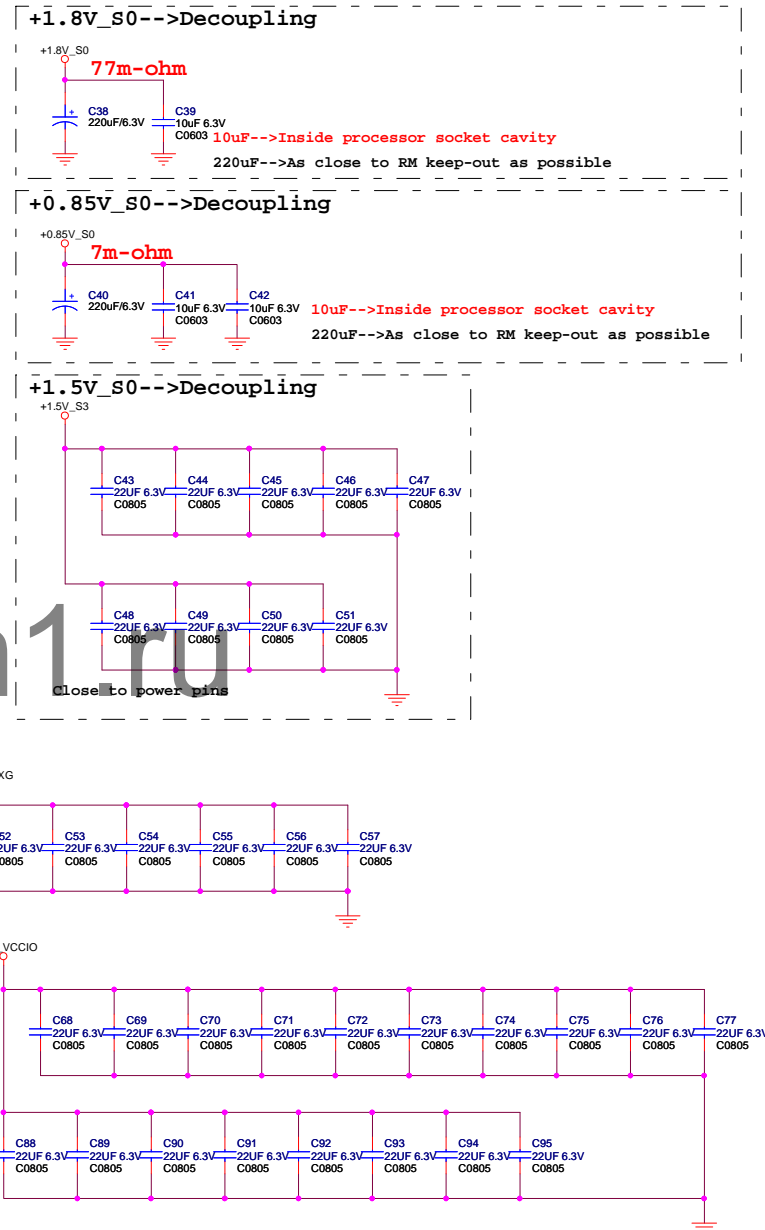
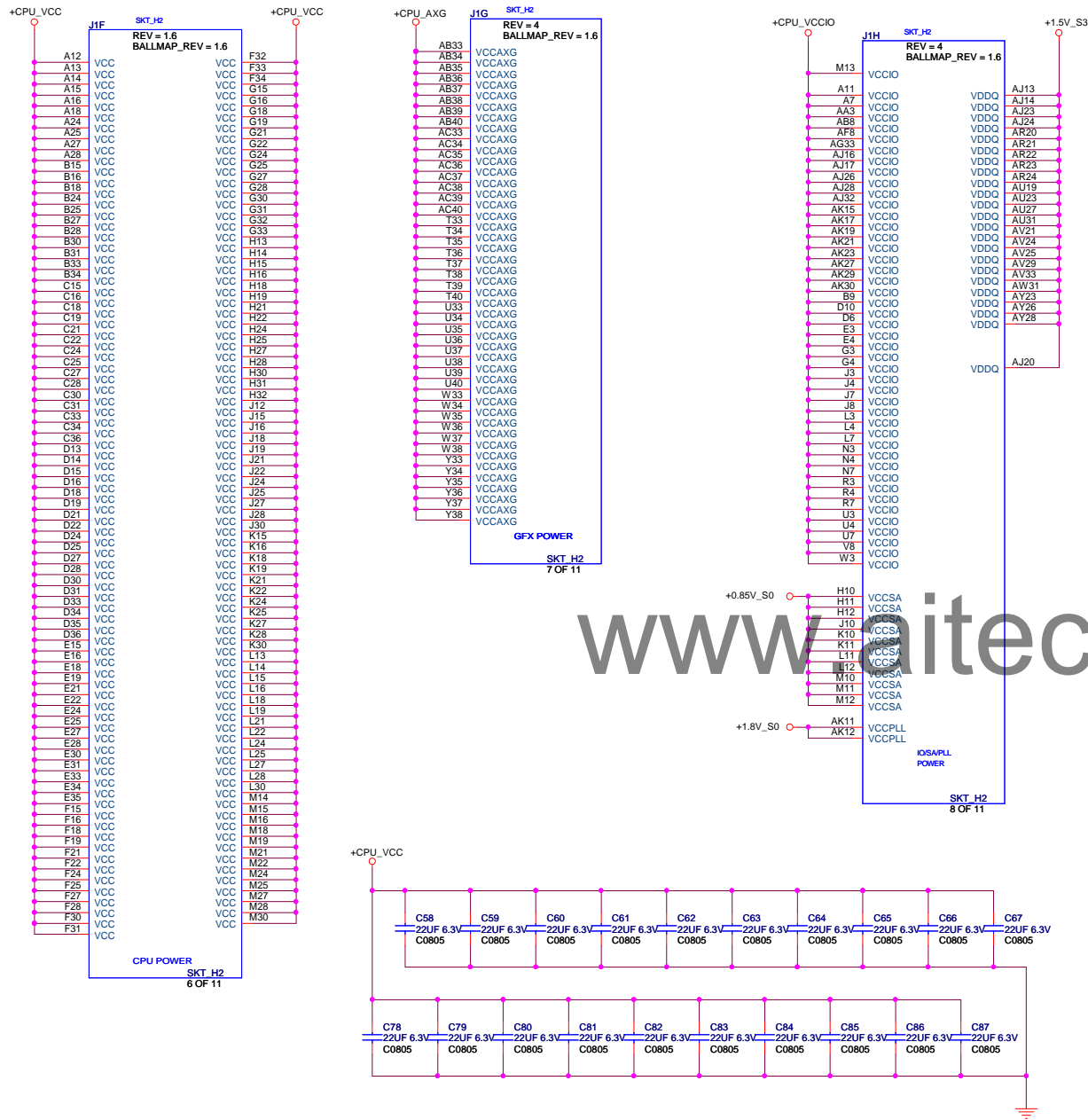


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev	ROA
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark	<remark>
Date	Thursday, December 22, 2011	Sheet	4 of 49		

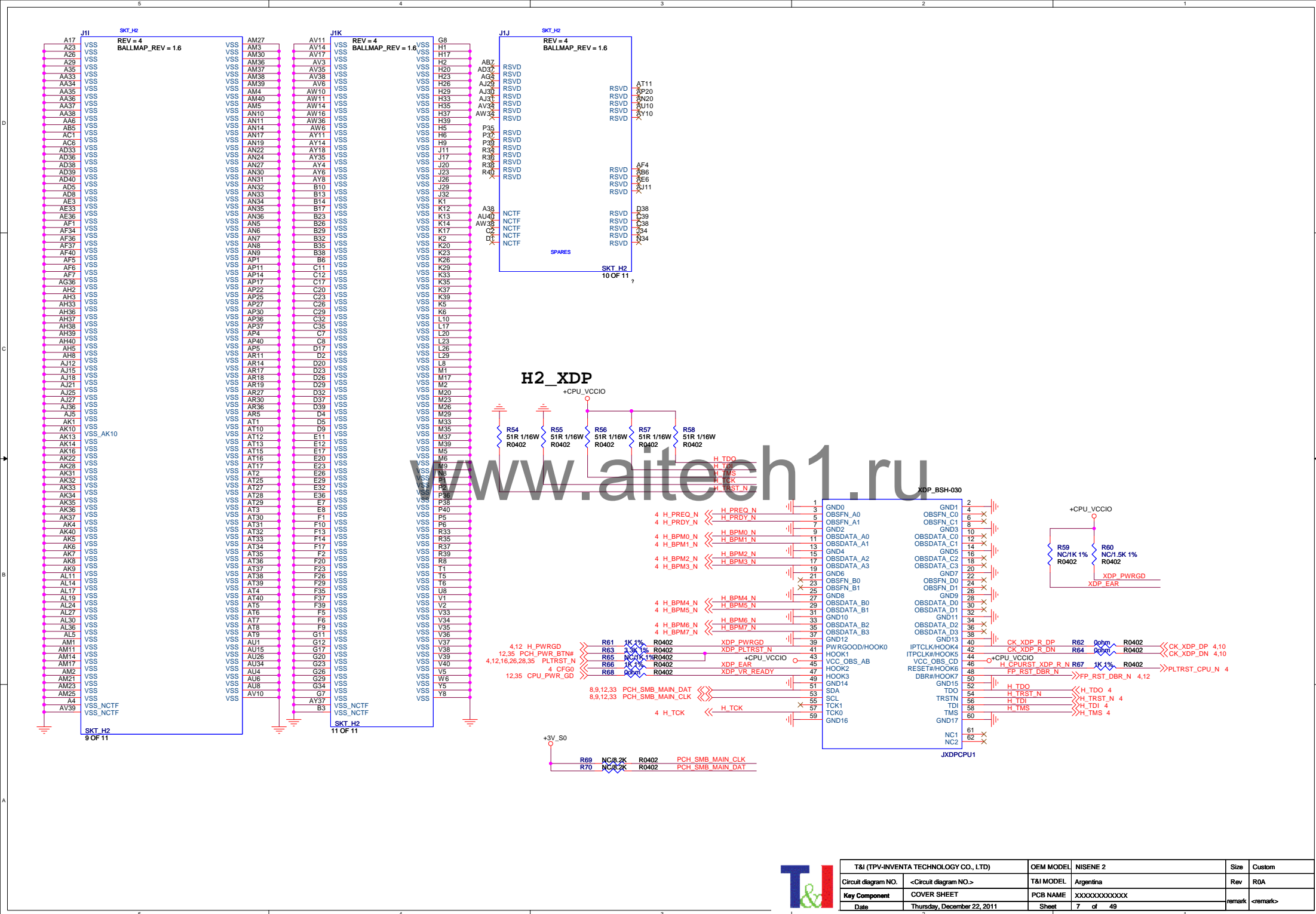


## Channel\_B

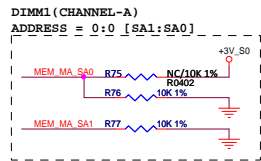
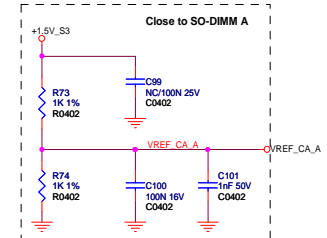
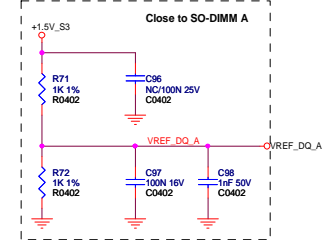
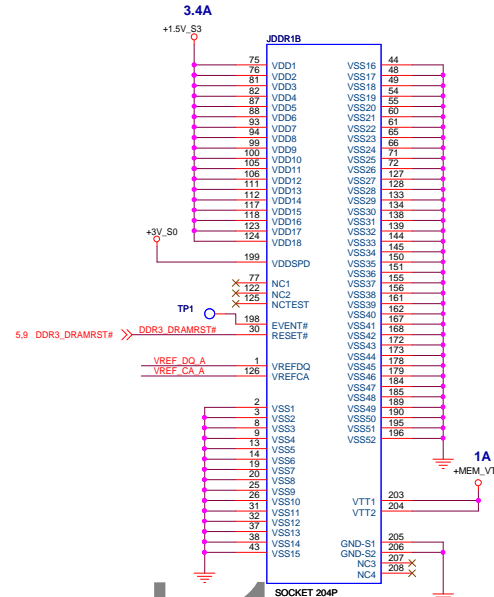




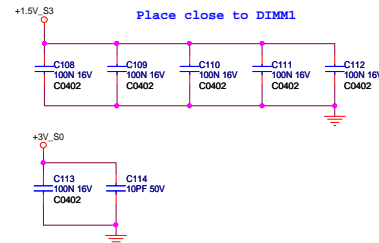
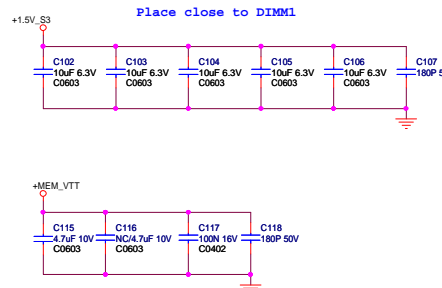
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	Custom
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Thursday, December 22, 2011	Sheet	6 of 49	<remark>



# CHA DDR 9.2H(DIMM-1)



Note:  
If SA0 = 0, SA1 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30  
If SA0 = 1, SA1 = 0  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32

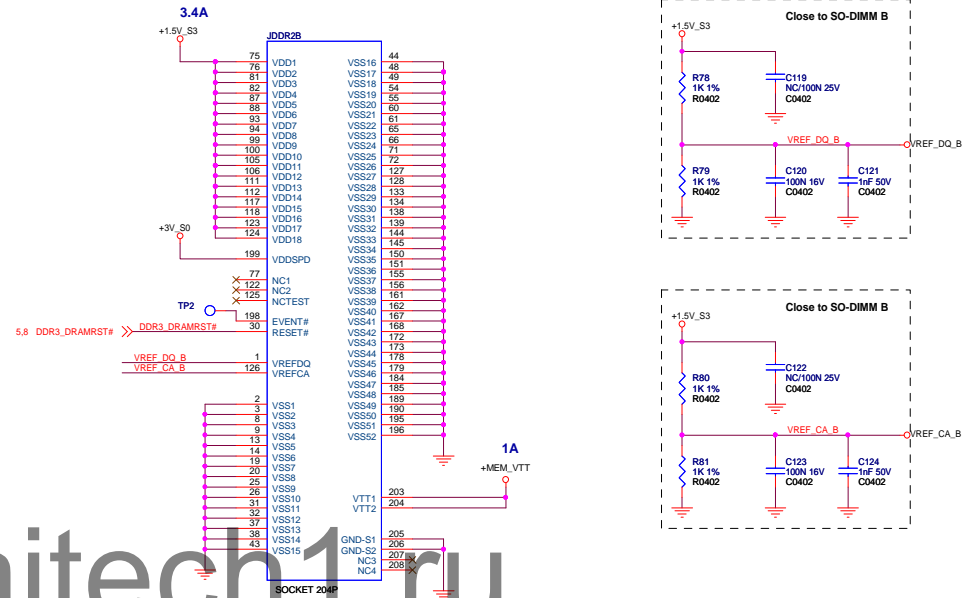
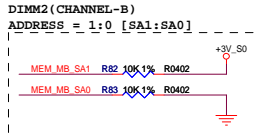


T&I (TPV-INTENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Thursday, December 22, 2011	Sheet	8 of 49	<remark>

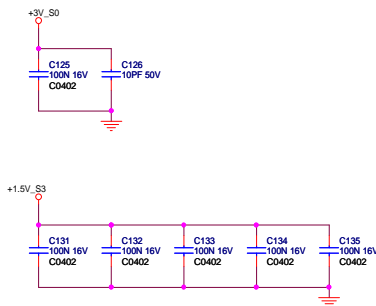
Pin 1 connection diagram for the SOCKET 204P. The diagram shows a 20-pin connector with the following connections:

- Pin 38: VSS13
- Pin 43: VSS14
- Pin 44: VSS15
- Pin 205: GND-S1
- Pin 206: GND-S2
- Pin 207: NC3
- Pin 208: NC4
- Pin 1: GND

SOCKET 204P

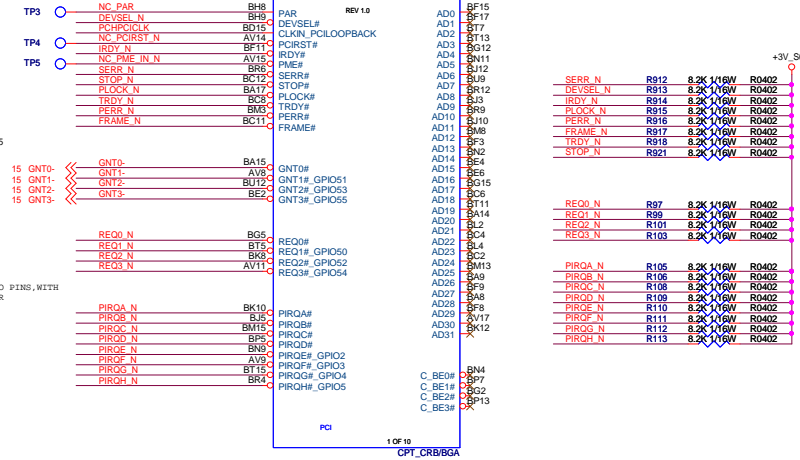


This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

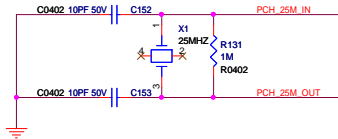


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev	RDA
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark	<remark>
Date	Thursday, December 22, 2011	Sheet	9 of 49		

*PCH\_PCI*



## XDP CONNECTOR



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev	ROA
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXXX	remark	<remark>
Date	Thursday, December 22, 2011	Sheet	10 of 49		

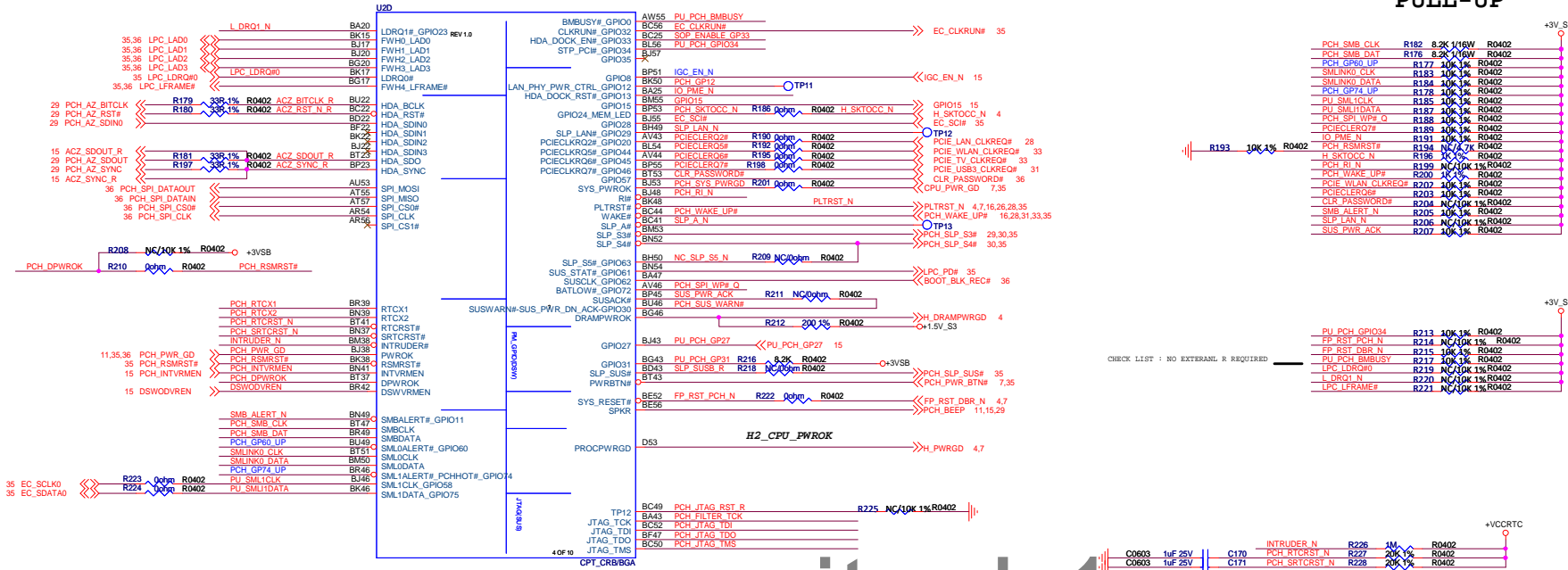






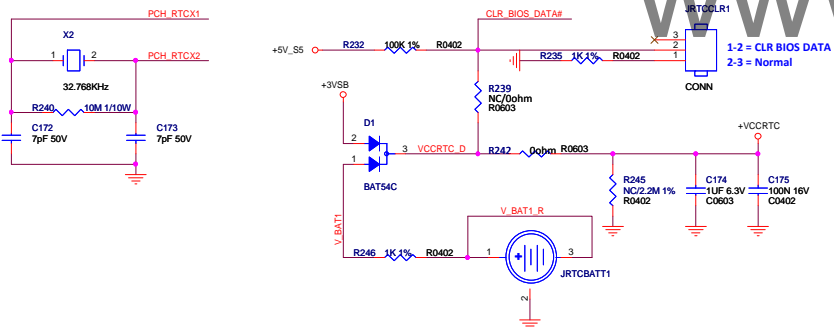
# PCH\_HDA/SPI/LPC/MISC/

# PULL-UP

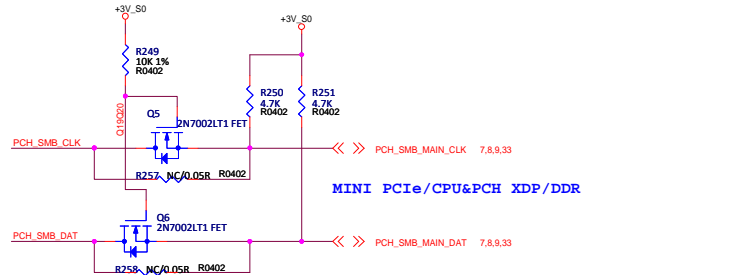


## RTC\_CLK

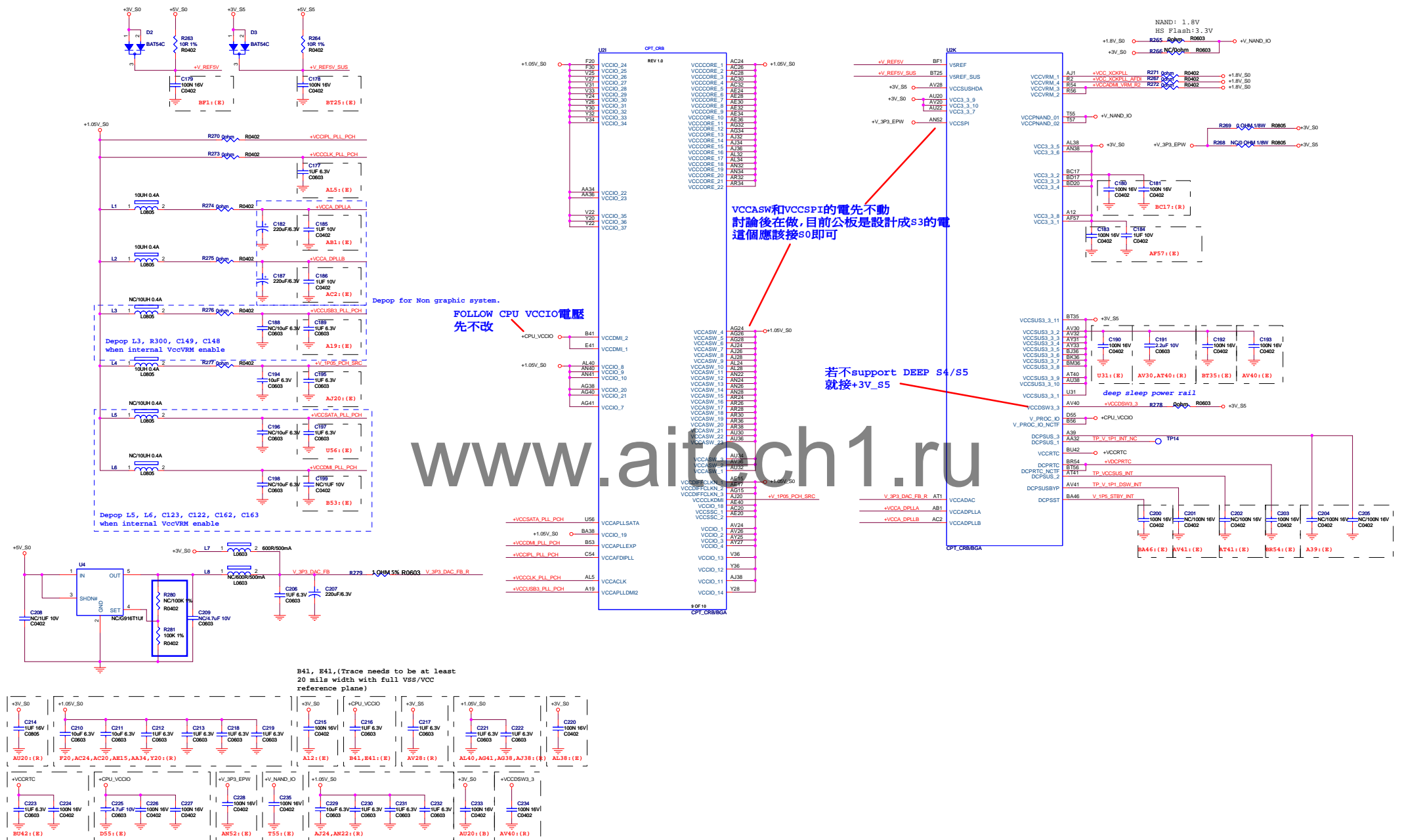
## RTC BATTERY & HP CLR BIOS DATA



## MINI PCIe/CPU&PCH XDP/DDR

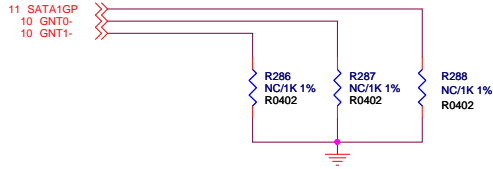


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	Rev
Date	Thursday, December 22, 2011	Sheet	12 of 49	remark



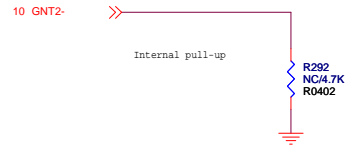


# CP REQUIRED STRAPS

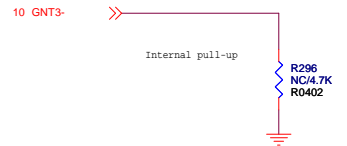


## BOOT select straps

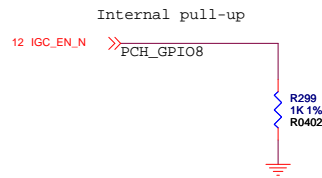
GNT1-	SATA1GP	Boot device
0	0	LPC
1	0	PCI
1	1	SPI(Default)



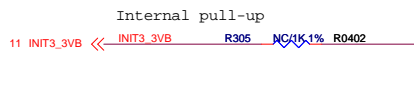
DMI AC/DC MODE  
0 : AC  
1 : DC \*



Topblock swap override when pull-low  
Signal has a weak internal pull-up

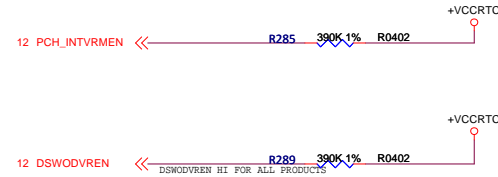


GPIO8  
0 : Integrated Clocking Enable (FCIM)\*  
1 : Buffer Through Mode Enable (BTM)



INT3\_3V#  
0 : ??????????????  
1 : ?????????????? \*

1: INIT3\_3V to asserted for 16 PCI clock to reset the processor by some evens occur.  
0: Can not to reset the processor.

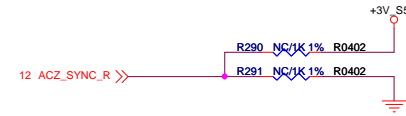


INTVRMEN  
0: DISABLE INTERNAL VRM  
1: ENABLE INTERNAL VRM \*

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN  
0 : Disable Internal Deep Sleep 1.05 V regulators.  
1 : Enable Internal Deep Sleep 1.05 V regulators.

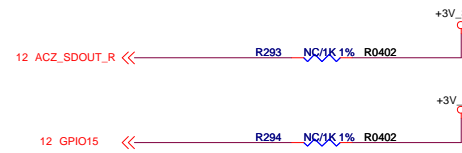
This signal enables the internal Deep Sleep 1.05 V regulators. Must be reconnected even when not supporting DSW.



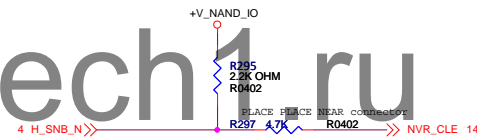
HDA\_SYNC  
OD PLL VR SUPPLY SEL  
0: 1.8V SUPPLY \*  
1: 1.5V SUPPLY

HDA\_SDO  
Disable ME in Manufacturing Mode  
when pull LOW ????

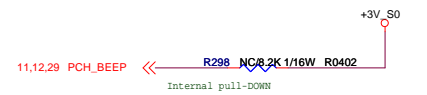
HDA\_SDO has internal pull down.  
Default should be connected to SDIN of codec, no pull up/down.  
To Disable ME need to have a jumper to pull high



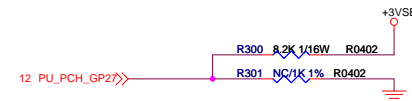
GPIO15  
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY \*  
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



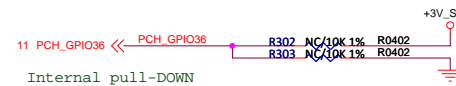
DMI/FDI TERMINATION VOLTAGE  
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH  
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW \*?  
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



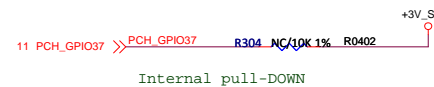
SPKR  
0 : EN TCO REBOOT \*  
1 : DIS TCO REBOOT



In Deep Sleep Power Well.  
If not used, require a weak pull-up(8.2k-10k) to VccDSW3\_3



Cougar point EDS PAGE:93 This signal should not be pull high



Cougar point EDS PAGE:93 This signal should not be pull high



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	Custom
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev R0A
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark <remark>
Date	Thursday, December 22, 2011	Sheet	15 of 49	

BOM Option

- UMA --> all don't stuff
- GPU --> all stuff

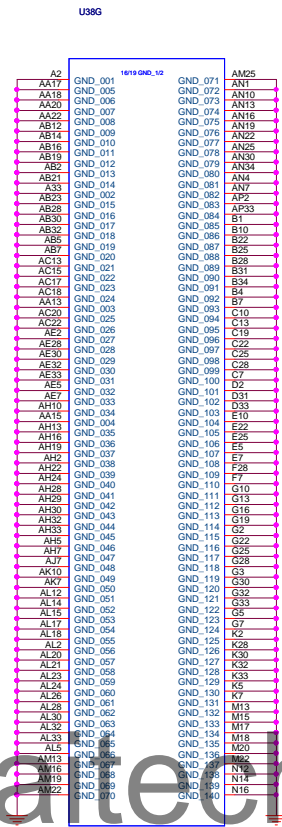
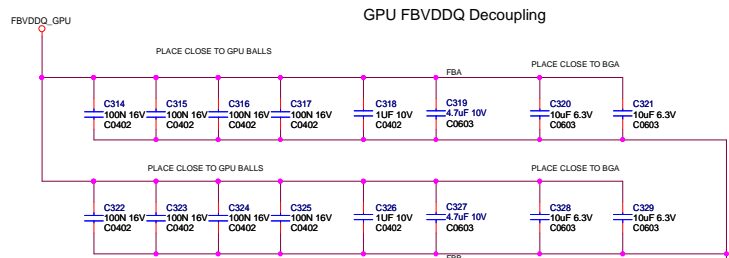
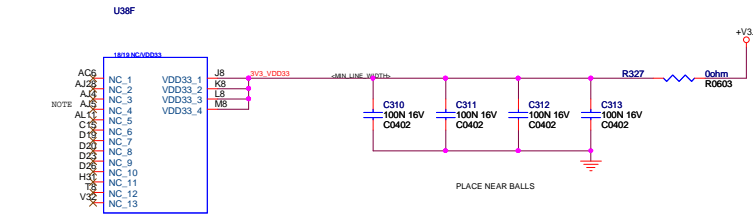
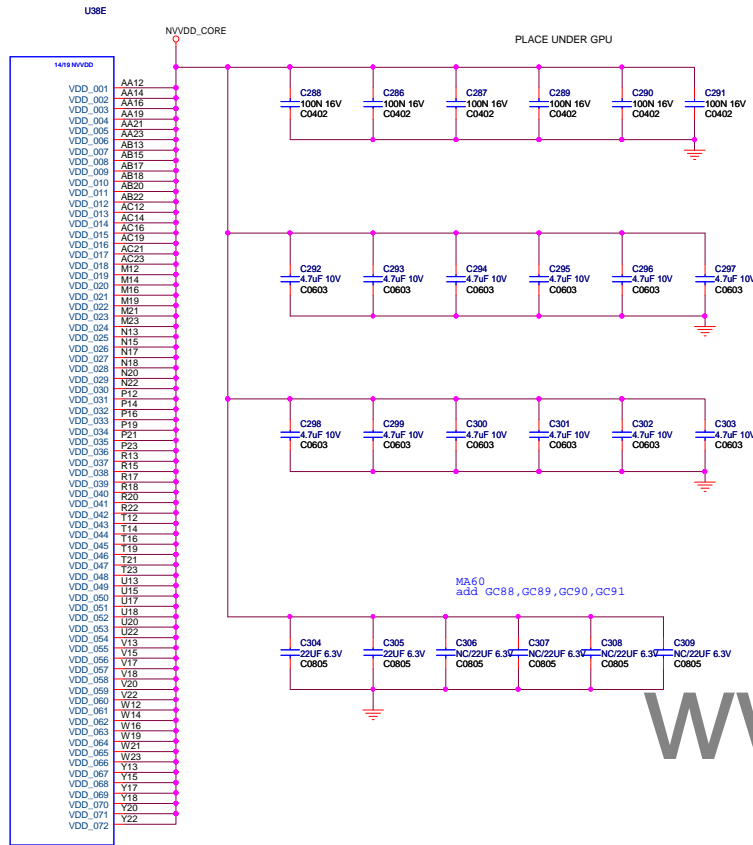


BOM Option  
UMA --> all don't stuff  
GPU --> all stuff

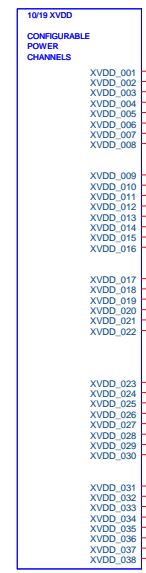
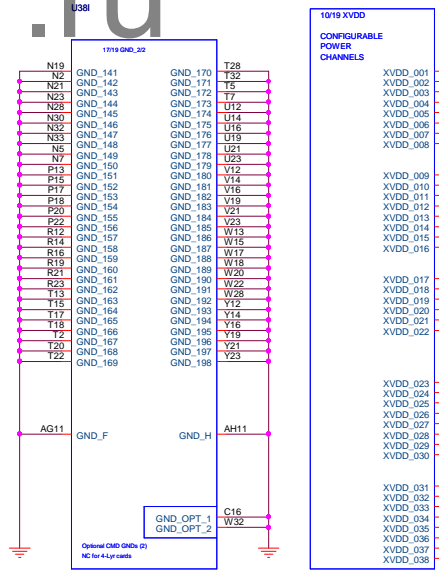
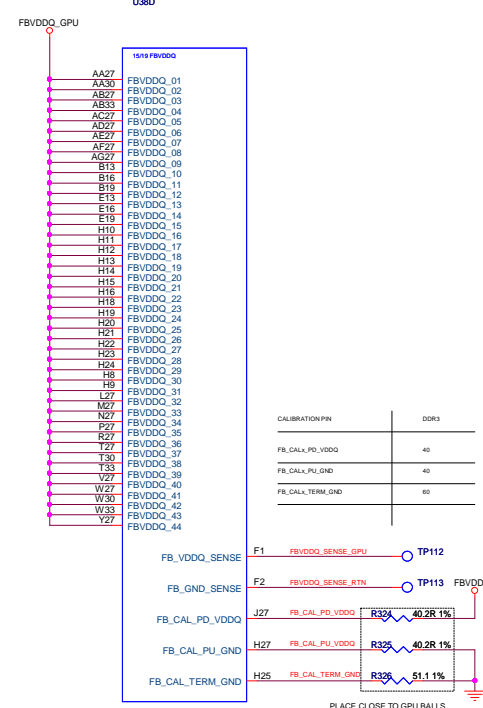


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2		Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina		Rev	ROA
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXXXXXX		remark	<remark>
Date	Thursday, December 22, 2011	Sheet	17 of 40			

# Power/Decoupling: NVVDD,3V3\_NV,GRND,and Optional

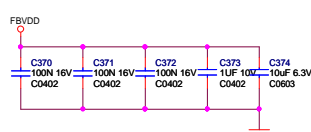
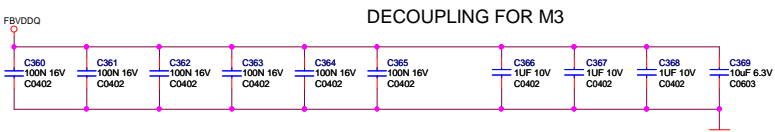
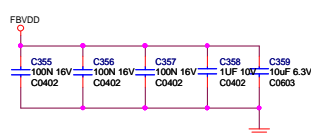
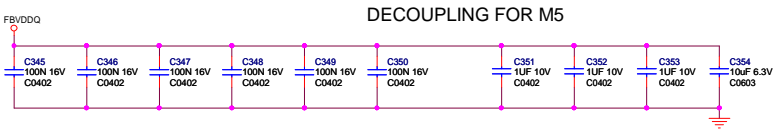
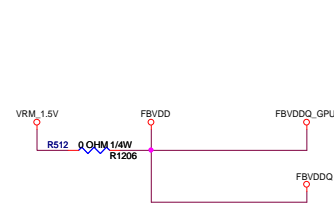
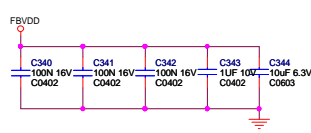
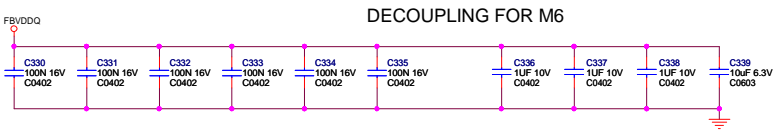


BOM Option  
UMA --> all don't stuff  
GPU --> all stuff

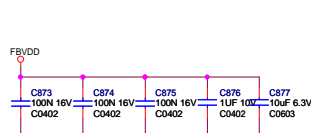
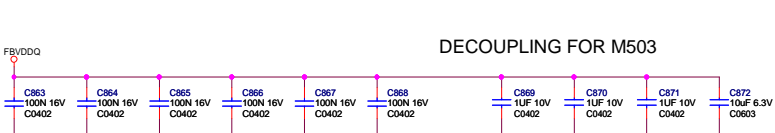
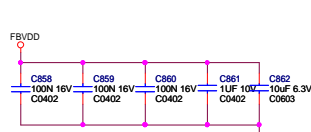
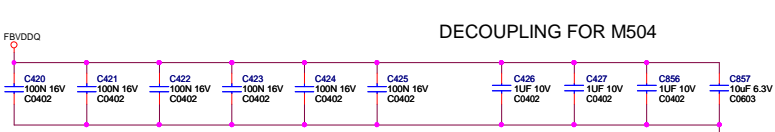
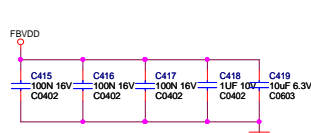
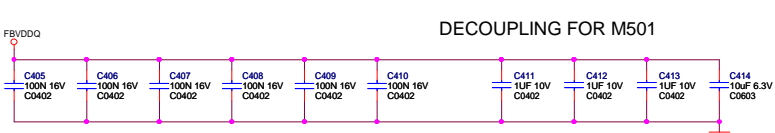
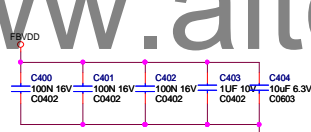
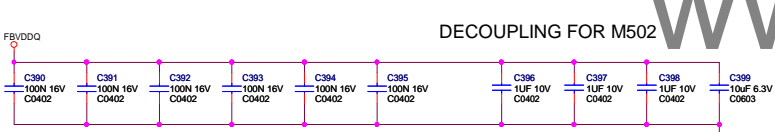
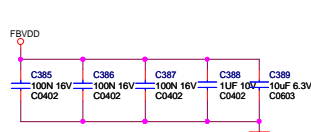
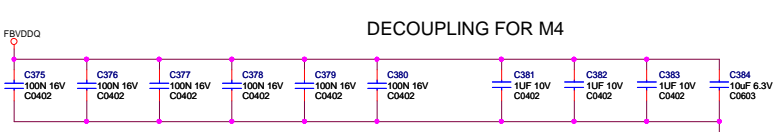


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL		Size	
Circuit diagram NO. <Circuit diagram NO.>		T&I MODEL		Rev	
Key Component		PCB NAME		remark	
Date		Sheet		18 of 49	





BOM Option  
UMA --> all don't stuff  
GPU --> all stuff

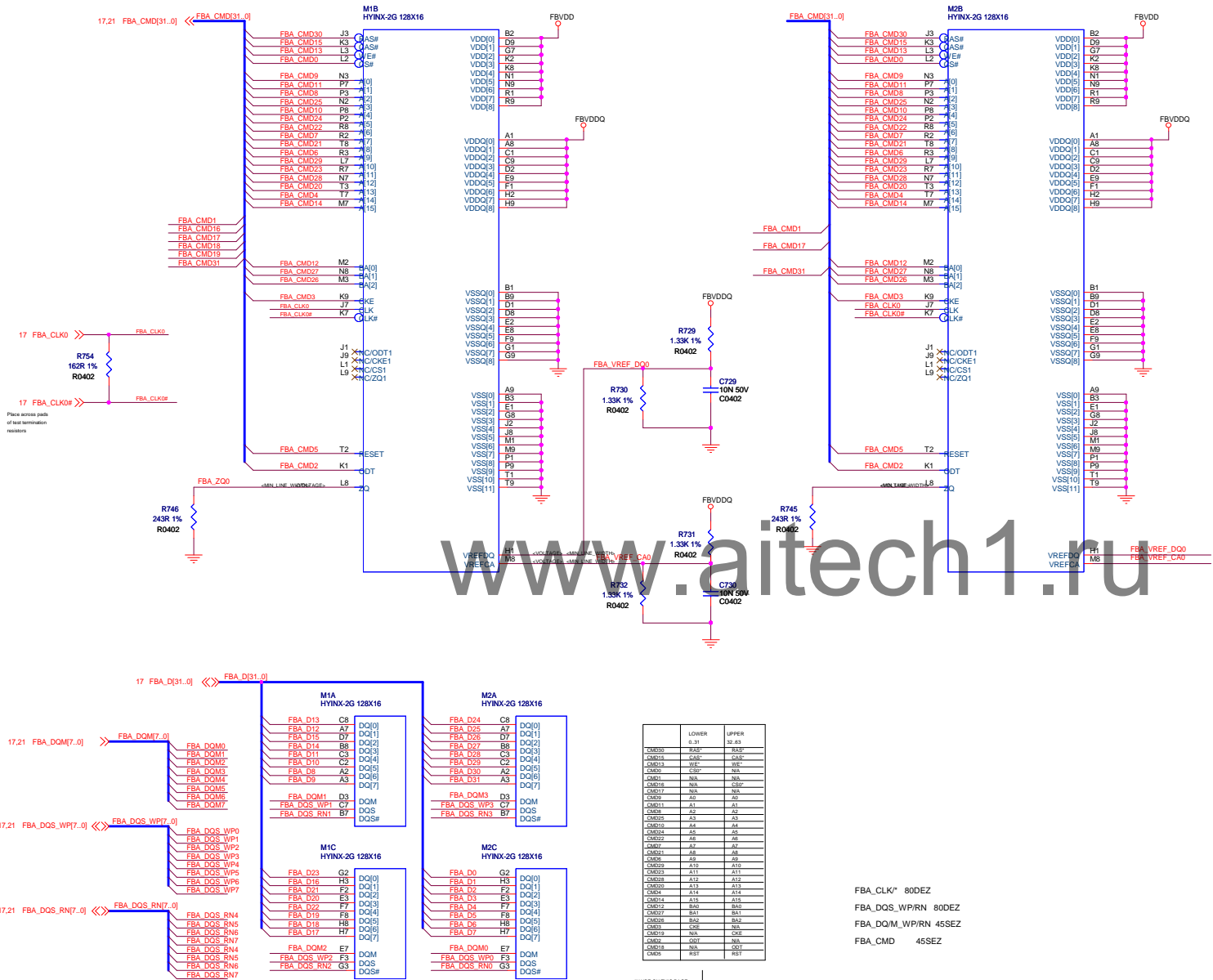


www.aitech1.ru



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	ROA
Date	Thursday, December 22, 2011	Sheet	19 of 49	remark

Memory Lower Partition A



- BOM Option
- UMA --> all don't stuff
  - GPU --> N13M-GE2 512MB, 16Mbx16 x4
  - GPU --> N13M-GE2 1GB, 16Mbx16 x8
  - GPU --> N13P-GT 1GB, 16Mbx16 x8
  - GPU --> N13P-GT 2GB, 128Mbx16 x8

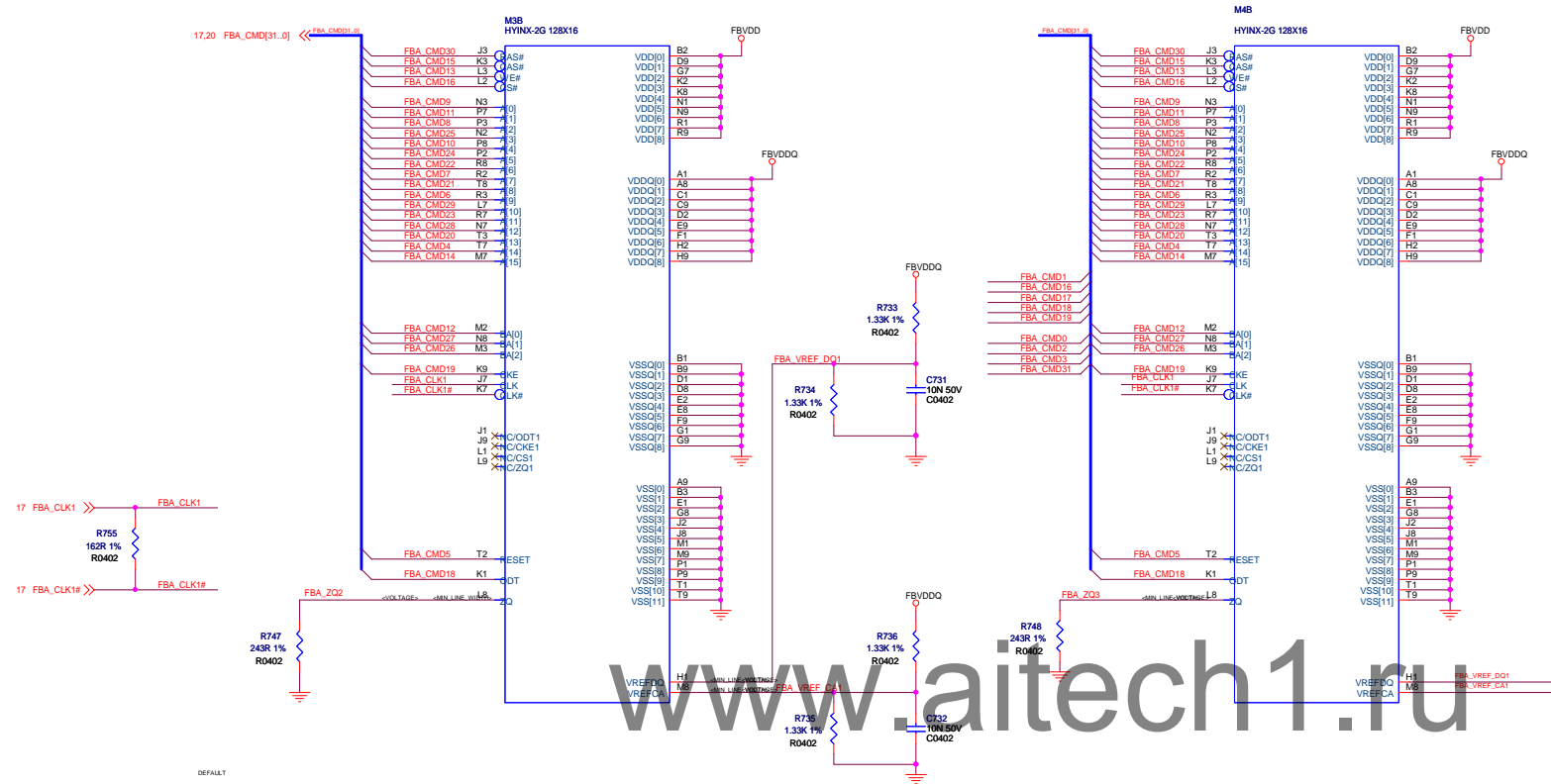
	LOWER	UPPER
CMD00	B0	B0
CMD01	B1	B1
CMD02	B2	B2
CMD03	B3	B3
CMD04	B4	B4
CMD05	B5	B5
CMD06	B6	B6
CMD07	B7	B7
CMD08	B8	B8
CMD09	B9	B9
CMD10	B10	B10
CMD11	B11	B11
CMD12	B12	B12
CMD13	B13	B13
CMD14	B14	B14
CMD15	B15	B15
CMD16	B16	B16
CMD17	B17	B17
CMD18	B18	B18
CMD19	B19	B19
CMD20	B20	B20
CMD21	B21	B21
CMD22	B22	B22
CMD23	B23	B23
CMD24	B24	B24
CMD25	B25	B25
CMD26	B26	B26
CMD27	B27	B27
CMD28	B28	B28
CMD29	B29	B29
CMD30	B30	B30
CMD31	B31	B31

FBA\_CLK# 80DEZ  
FBA\_DQS\_WP/RN 80DEZ  
FBA\_DQ/M\_WP/RN 45SEZ  
FBA\_CMD 45SEZ



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO. <Circuit diagram NO.>	T&I MODEL	Argentina	Rev	ROA
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark <remark>
Date	Thursday, December 22, 2011	Sheet	20	of 49

Memory Upper Partition A



BOM Option  
UMA --> all don't stuff  
GPU --> N13M-GE2 512MB , 16Mbx16 x4  
GPU --> N13M-GE2 1GB , 16Mbx16 x8  
GPU --> N13P-GT 1GB , 16Mbx16 x8  
GPU --> N13P-GT 2GB , 128Mbx16 x8

www.aitech1.ru

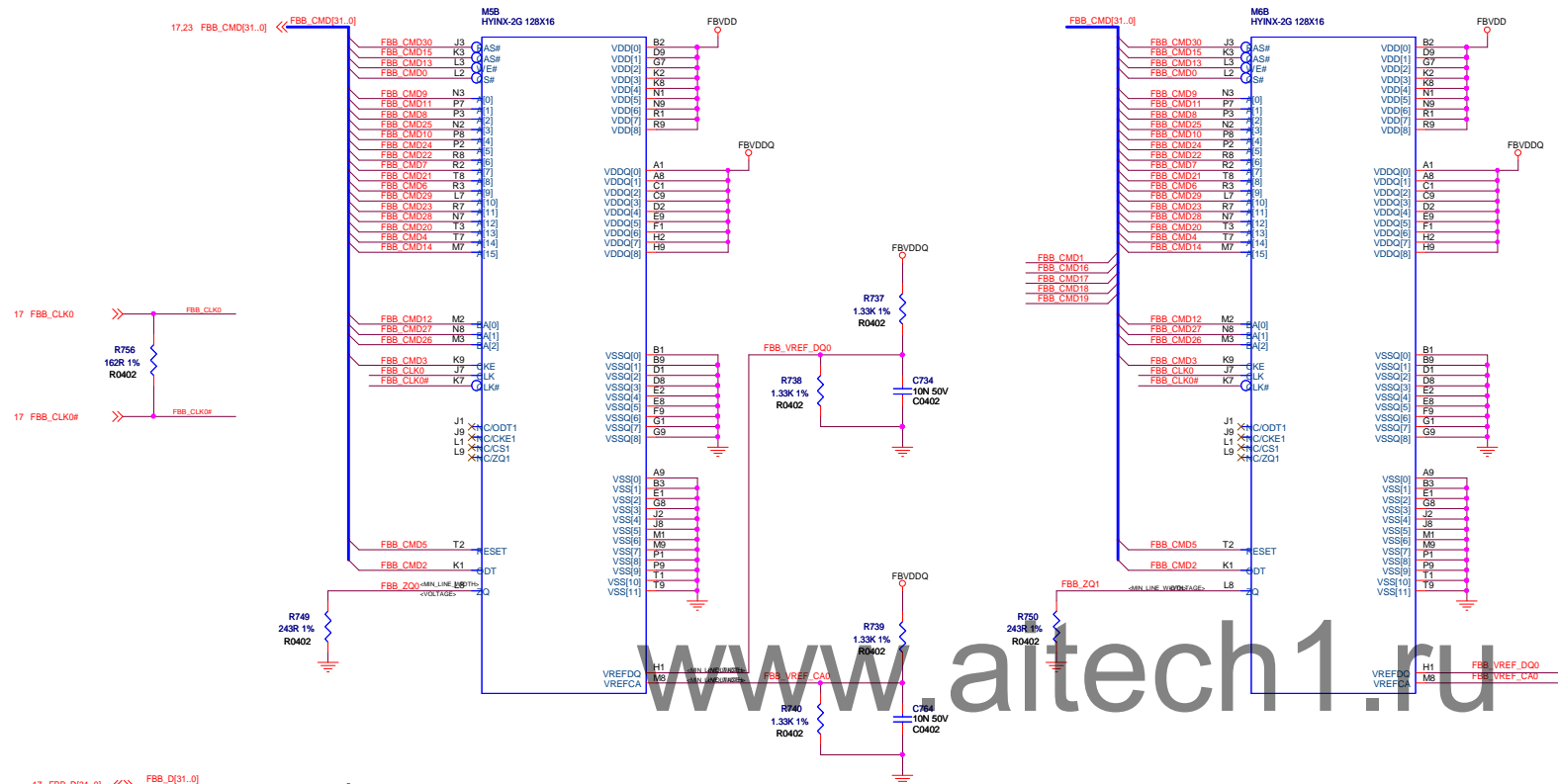
	LOWER	UPPER
CM000	BA0*	BA0*
CM019	CA0*	CA0*
CM013	WE*	WE*
CM018	CS0*	CS0*
CM01	NA	NA
CM016	NA	NA
CM017	NA	NA
CM011	A1	A1
CM010	AS	AS
CM009	A3	A3
CM008	AS	AS
CM004	A5	A5
CM002	AS	AS
CM007	A7	A7
CM001	AS	AS
CM006	AS	AS
CM020	A10	A10
CM003	A11	A11
CM028	A12	A12
CM005	A15	A15
CM04	A14	A14
CM014	A15	A15
CM012	BA0	BA0
CM007	BA1	BA1
CM026	BA2	BA2
CM03	CA0	CA0
CM019	NA	CA0
CM018	NA	CA0
CM025	BA0	BA0

INUSE ON THIS PAGE



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO. <Circuit diagram NO.>	T&I MODEL	Argentina	Rev	ROA
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark <remark>
Date	Thursday, December 22, 2011	Sheet	21	of 49

## Memory Lower Partition B



BOM Option

UMA --> all don't stuff

GPU --> N13M-GE2 512MB, 16Mbx16 x4

GPU --> N13M-GE2 1GB, 16Mbx16 x8

GPU --> N13P-GT 1GB, 16Mbx16 x8

GPU --> N13P-GT 2GB, 128Mbx16 x8

www.aitech1.ru

	LOWER	UPPER
CM205	D0E	D0E
CM206	D0E	D0E
CM207	D0E	D0E
CM208	D0E	D0E
CM209	D0E	D0E
CM210	D0E	D0E
CM211	D0E	D0E
CM212	D0E	D0E
CM213	D0E	D0E
CM214	D0E	D0E
CM215	D0E	D0E
CM216	D0E	D0E
CM217	D0E	D0E
CM218	D0E	D0E
CM219	D0E	D0E
CM220	D0E	D0E
CM221	D0E	D0E
CM222	D0E	D0E
CM223	D0E	D0E
CM224	D0E	D0E
CM225	D0E	D0E
CM226	D0E	D0E
CM227	D0E	D0E
CM228	D0E	D0E
CM229	D0E	D0E
CM230	D0E	D0E
CM231	D0E	D0E
CM232	D0E	D0E
CM233	D0E	D0E
CM234	D0E	D0E
CM235	D0E	D0E
CM236	D0E	D0E
CM237	D0E	D0E
CM238	D0E	D0E
CM239	D0E	D0E
CM240	D0E	D0E

FBA\_CLK\* 80DEZ

FBA\_DQS\_WP/RN 80DEZ

FBA\_DQM\_WP/RN 45SEZ

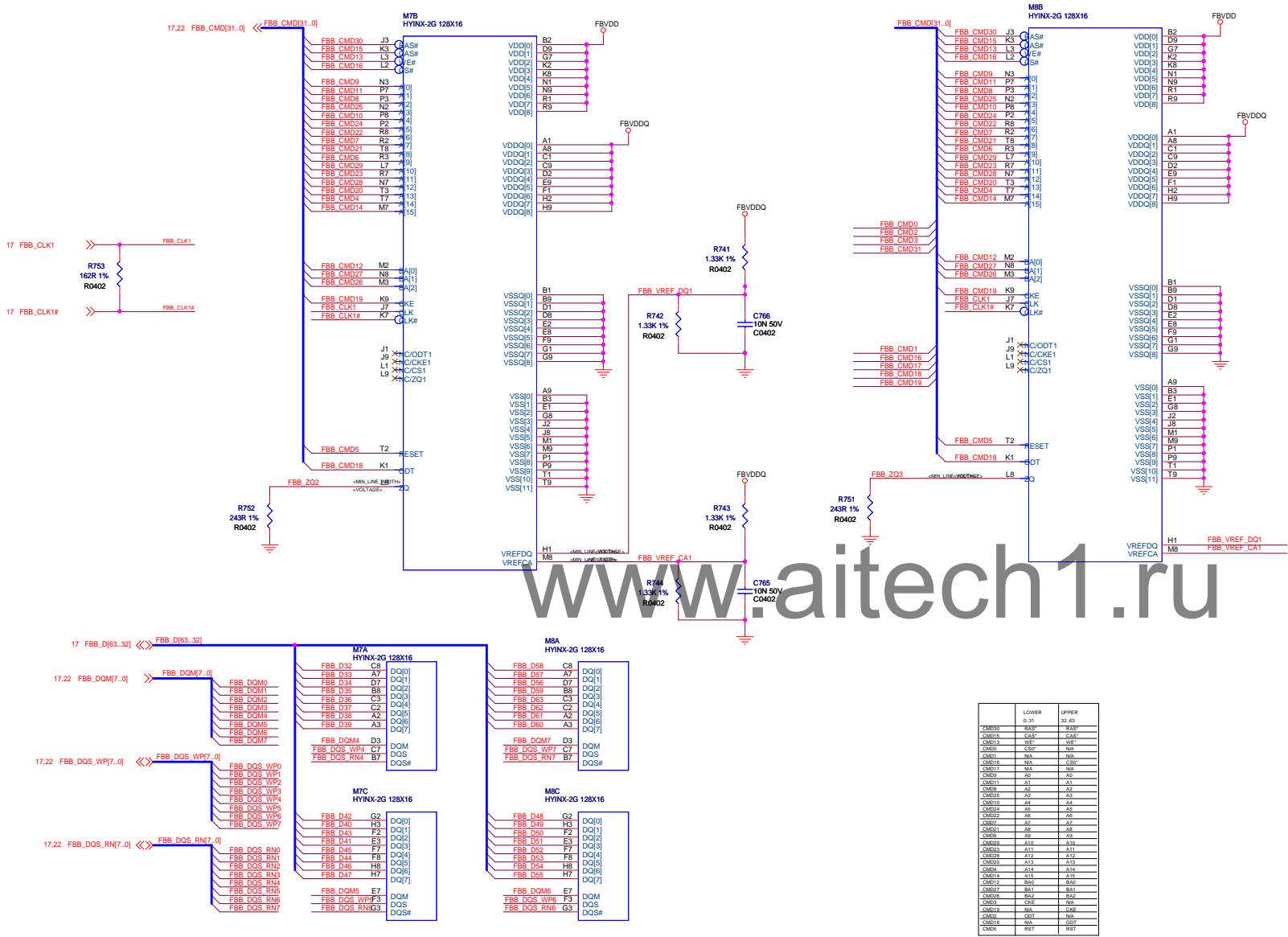
FBA\_CMD 45SEZ

IN USE ON THIS PAGE



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO. <Circuit diagram NO.>	T&I MODEL	Argentina	Rev	ROA
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark <remark>
Date	Thursday, December 22, 2011	Sheet	22 of 49	

Memory Upper Partition B



BOM Option  
UMA --> all don't stuff  
GPU --> N13M-GE2 512MB , 16Mbx16 x4  
GPU --> N13M-GE2 1GB , 16Mbx16 x8  
GPU --> N13P-GT 1GB , 16Mbx16 x8  
GPU --> N13P-GT 2GB , 128Mbx16 x8

	LOWER 0-31	UPPER 32-63
FBB_DQ0	DATA0	DATA0
FBB_DQ1	DATA1	DATA1
FBB_DQ2	DATA2	DATA2
FBB_DQ3	DATA3	DATA3
FBB_DQ4	DATA4	DATA4
FBB_DQ5	DATA5	DATA5
FBB_DQ6	DATA6	DATA6
FBB_DQ7	DATA7	DATA7
FBB_DQ8	DATA8	DATA8
FBB_DQ9	DATA9	DATA9
FBB_DQ10	DATA10	DATA10
FBB_DQ11	DATA11	DATA11
FBB_DQ12	DATA12	DATA12
FBB_DQ13	DATA13	DATA13
FBB_DQ14	DATA14	DATA14
FBB_DQ15	DATA15	DATA15
FBB_DQ16	DATA16	DATA16
FBB_DQ17	DATA17	DATA17
FBB_DQ18	DATA18	DATA18
FBB_DQ19	DATA19	DATA19
FBB_DQ20	DATA20	DATA20
FBB_DQ21	DATA21	DATA21
FBB_DQ22	DATA22	DATA22
FBB_DQ23	DATA23	DATA23
FBB_DQ24	DATA24	DATA24
FBB_DQ25	DATA25	DATA25
FBB_DQ26	DATA26	DATA26
FBB_DQ27	DATA27	DATA27
FBB_DQ28	DATA28	DATA28
FBB_DQ29	DATA29	DATA29
FBB_DQ30	DATA30	DATA30
FBB_DQ31	DATA31	DATA31

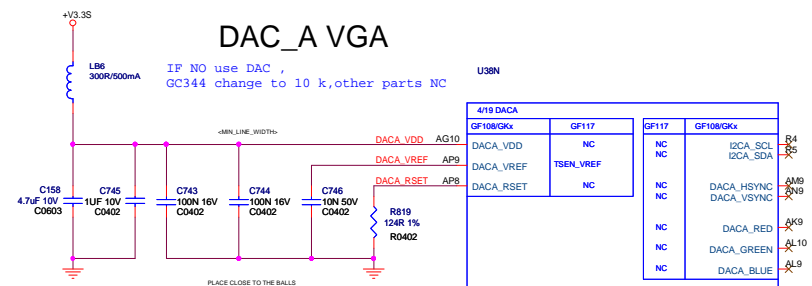
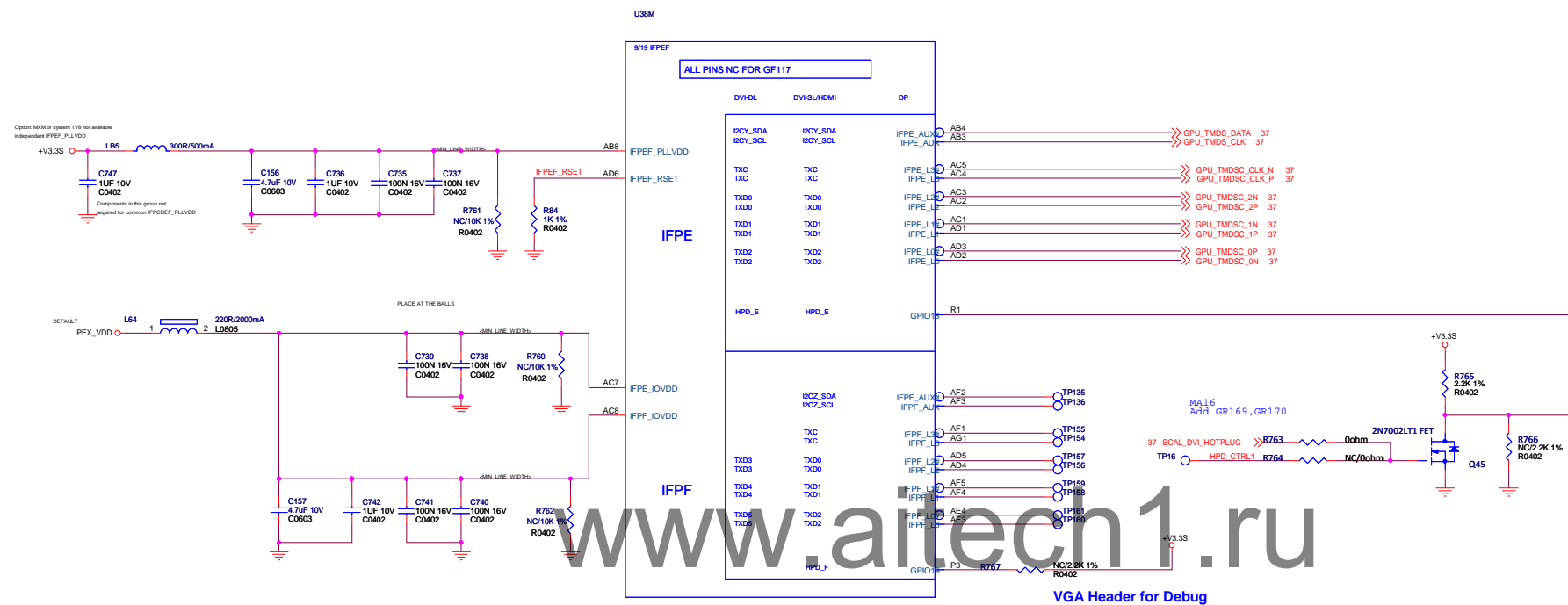
INCLUDE ON  
THIS PAGE



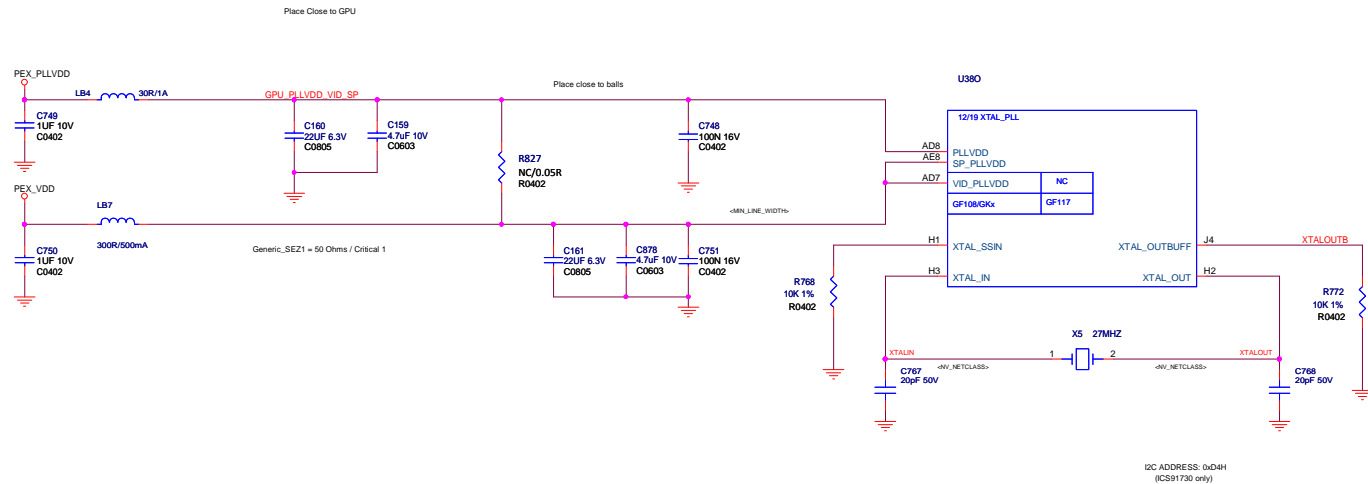
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev	ROA
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark	<remark>
Date	Thursday, December 22, 2011	Sheet	23 of 49		

UMA --> all don't stuff  
GPU --> IFPE : DVI OUT for PC

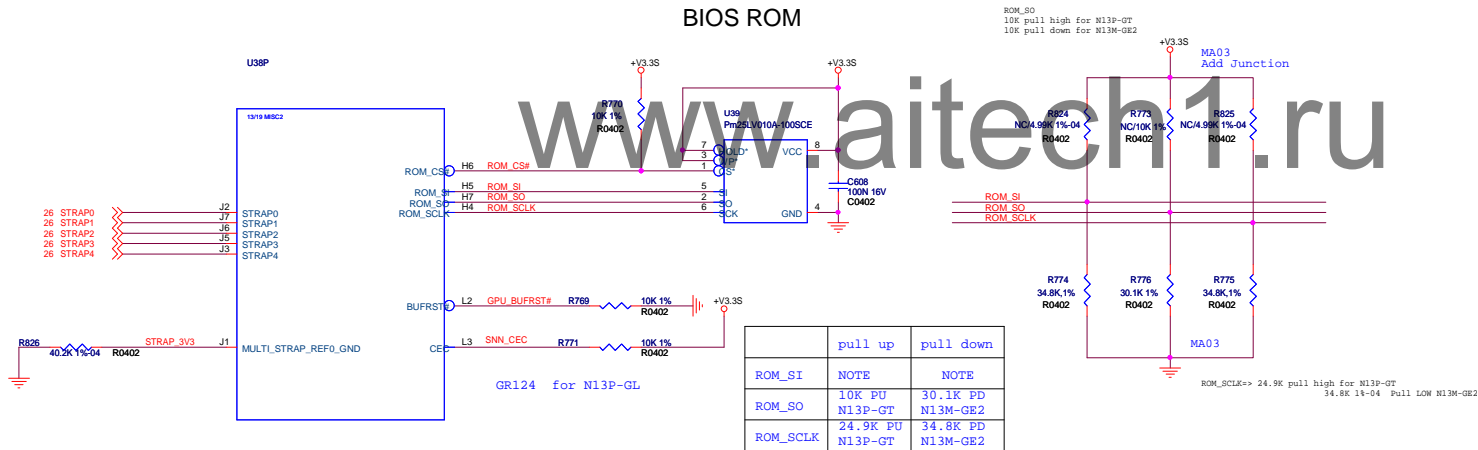
## IFPE/F Dual Link TMDS DVI-I



## BIOS, External SS, and Mechanical Components



## BIOS ROM



	pull up	pull down
ROM_SI	NOTE	NOTE
ROM_SO	10K PU N13P-GT	30.1K PD N13M-GE2
ROM_SCLK	24.9K PU N13P-GT	34.8K PD N13M-GE2

BOM Option  
UMA --> all don't stuff  
GPU --> Please refer to left table to configure N13x-xx

PIN NAME	MULTI-LEVEL	BINARY PRODUCTION	BINARY BRINGUP
MULTI_STRAP_REF_GND	40.2K TO GND	NO STUFF	NOT SUPPORTED

GF117/GK10X STRAPPING MODE TABLE			
PIN NAME	MULTI-LEVEL	BINARY PRODUCTION	BINARY BRINGUP
MULTI_STRAP_REF_GND	40.2K TO GND	NOT SUPPORTED	NO STUFF

```
NOTE N13P-GT/GS
128X16 DDR3 samsung 0X7 K4W2G1646C-HC11
PD 45.3K
64X16 DDR3 samsung 0X3 K4W1G1646G-BC11
PD 20K

128X16 DDR3 Hynix 0X6 H5TQ2G63BFR-11C
PD 34.8K
64X16 DDR3 Hynix 0X2 H5TQ1G63DFR-11C
PD 15K
```

```
NOTE N13M-GE2
128X16 DDR3  samsung 0X7 K4W2G1646C-HC11
PD 45.3K
64X16 DDR3  samsung 0X3 K4W1G1646G-BC11
PD 20K

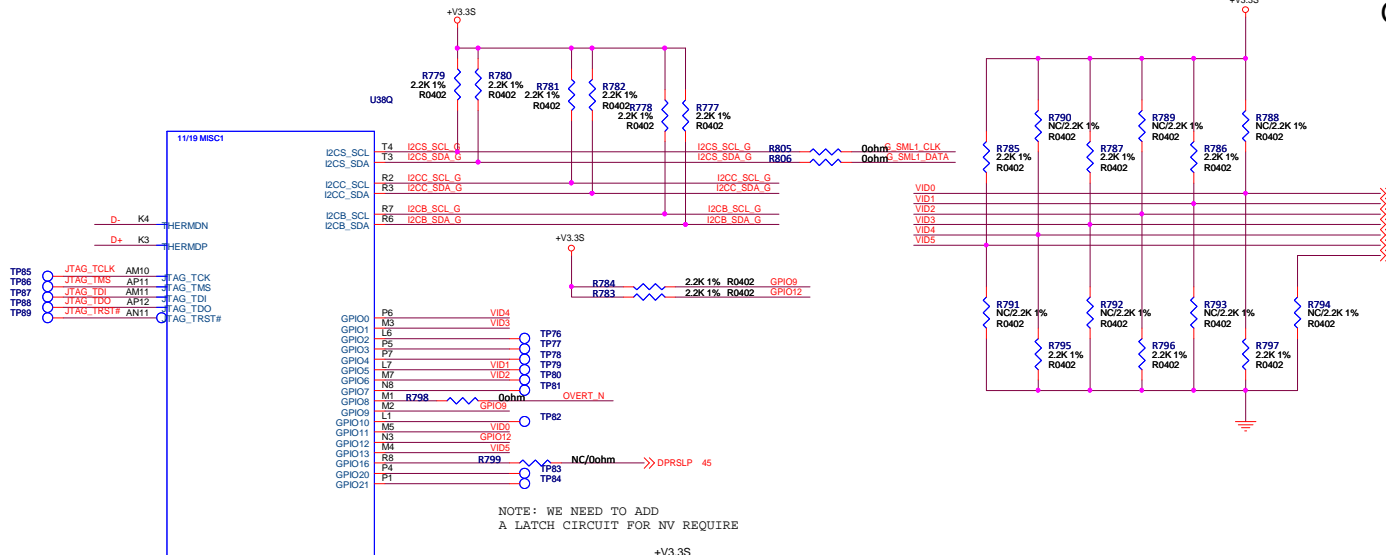
128X16 DDR3  Hynix 0X6 H5TQ2G63BFR-11C
PD 34.8K
64x16 DDR3  Hynix 0X2 H5TG1G63DFR-11C
PD 15K
```



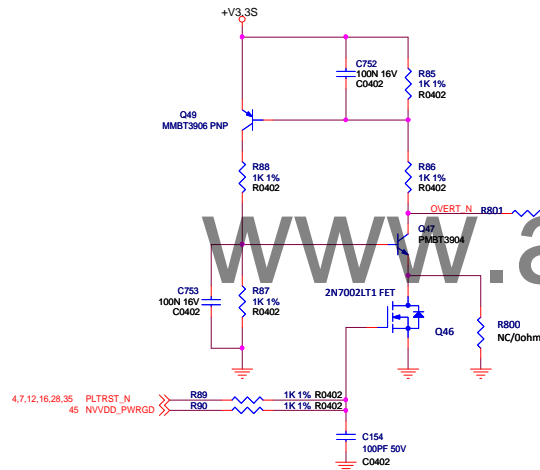
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2		Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina		Rev	ROA
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXXXXXX			
Date	Thursday, December 22, 2011	Sheet	26 of 40		remark	<remark>



# GPIOs, Thermal Sensor, I2C/GPIO Expanders



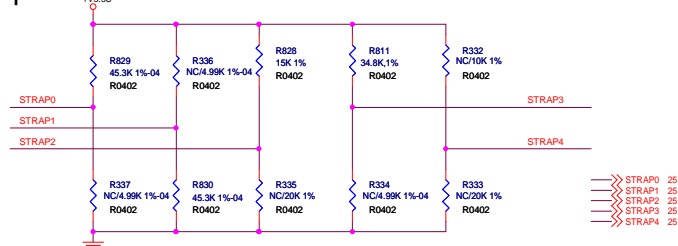
	pull up	pull down
STARP0	GR133 PU 45.3K	
STARP1		GR139 PD 34.8K
STARP2	GR135 15k PU N13M-GE2	GR140 10k PD N13P-GT
STARP3	GR136 PU 34.8K 1110	
STARP4		GR142 PD GR142 NC N13P-GT N13M-GE2



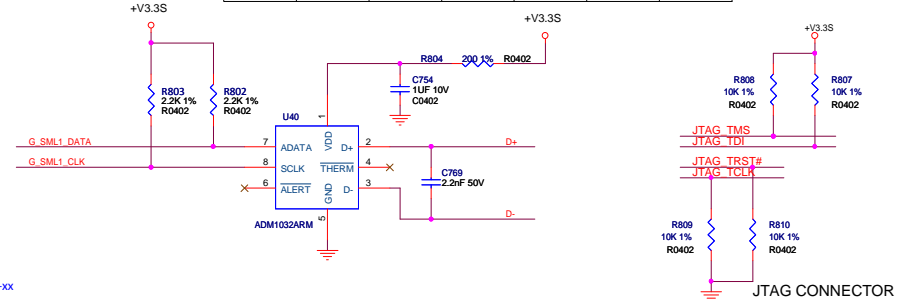
VID6	VID5	VID4	VID3	VID2	VID1	VID0
0	1	0	1	0	1	0
0	1	0	1	1	0	0

0,975V N13P-GT DEFAULT  
0,95V N13M-GE2

## Straps



BOM Option  
UMA -> all don't stuff  
GPU -> Please refer to below table to configure N13x-xx



GF117/GK10X STRAP PIN MODE TABLE

PIN NAME	MULTI-LEVEL bit [3:0]	BINARY PRODUCTION	BINARY BRINGUP
STRAP0	USER[3:0]		3GIO_PADCFG_LUT_ADR0
STRAP1	3GIO_PADCFG_ADR[3:0]		3GIO_PADCFG_LUT_ADR1
STRAP2	PCI_DEVID[3:0]		3GIO_PADCFG_LUT_ADR2
STRAP3	SOR[3:0]_EXPOSED		3GIO_PADCFG_LUT_ADR3
STRAP4	RSV, RSV, PCIE_MAX_SPEED, DP_PLL_VDD33V		PCIE_MAX_SPEED
ROM_SCLK	DEVID[4], SUB_VENDOR, DEVID[5], PEX_PLL_EN_TERM		SMB_ALT_ADDR
ROM_SI	RAMCFG[3:0]		SUB_VENDOR
ROM_SO	FB[1]_BAR_SIZE, FB[0]_BS, SMB_ALT_ADDR, VGA_DEVICE		VGA_DEVICE

GF108 STRAP PIN MODE TABLE

PIN NAME	MULTI-LEVEL bit [3:0]	BINARY PRODUCTION	BINARY BRINGUP
STRAP0	USER[3:0]		RAMCFG0
STRAP1	3GIO_PADCFG_ADR[3:0]		RAMCFG1
STRAP2	PCI_DEVID[3:0]		RAMCFG2
ROM_SCLK	PCIDEVID[4], SUB_VENDOR, SLOT_CLK, PEX_PLL_EN_TERM		PCI_DEVID3
ROM_SI	RAMCFG[3:0]		PCI_DEVID_EXT
ROM_SO	XCLK_417, FB0_BAR_SIZE, SMB_ALT_ADDR, VGA_DEVICE		XCLK_417

NOTE 2: See table 1 for the correct value/location of the strap resistor for the desired modes

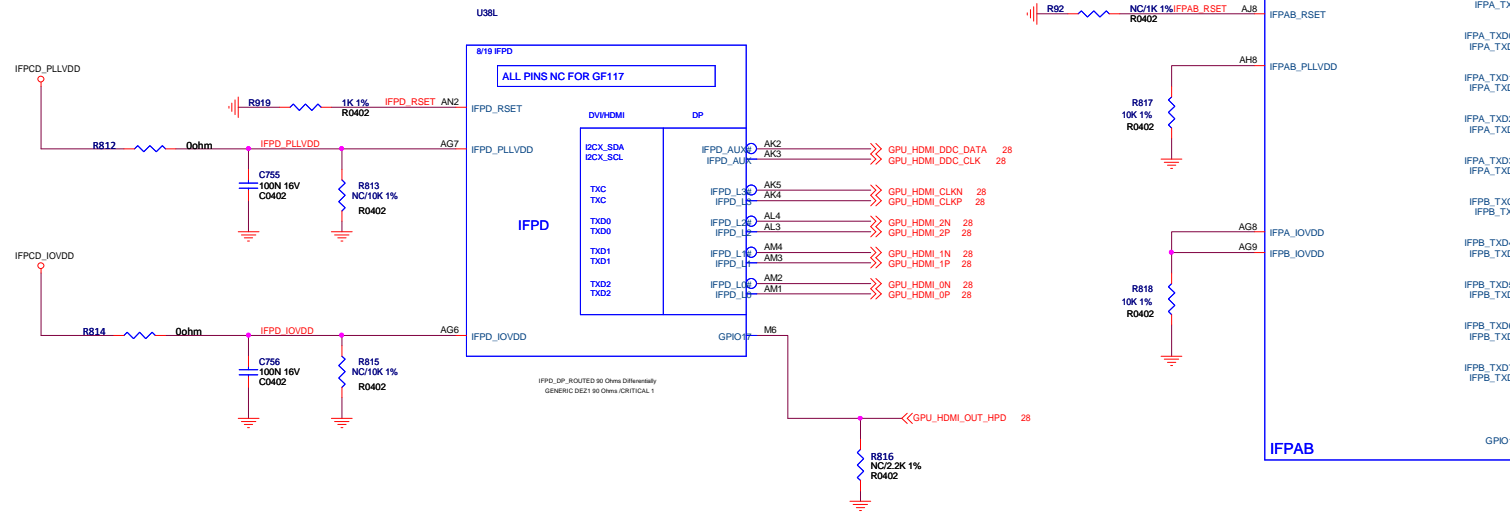
NOTE 3: Bring-up SKU(s) have jumper configurable subvendor and DEVID\_4 settings see the ROM\_SCLK STRAP



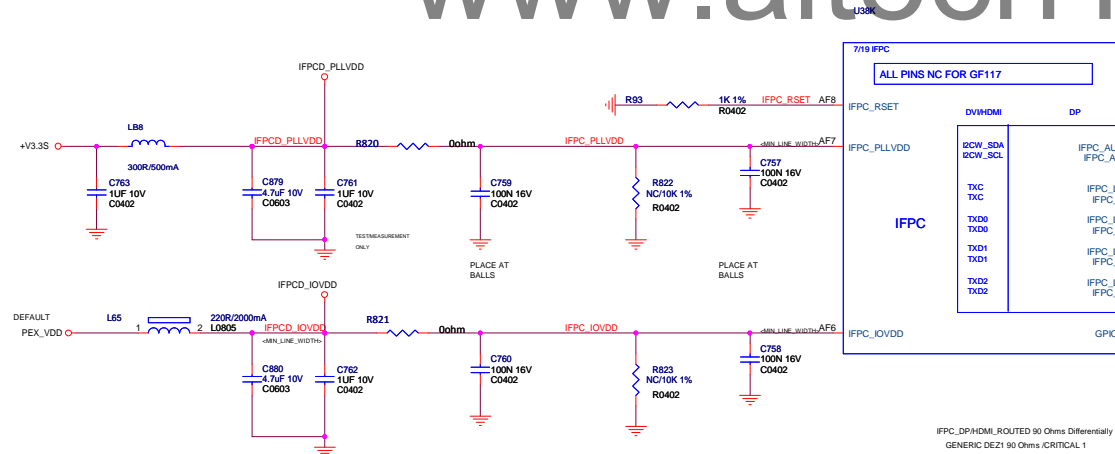
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Thursday, December 22, 2011	Sheet	26 of 49	

UMA --> all don't stuff  
BOM Option  
GPU --> IFPD : HDMI OUT for TV  
GPU --> IFPC : HDMI OUT for External HDMI out

## IFPA/B LVDS Dual Link



www.aitech1.ru

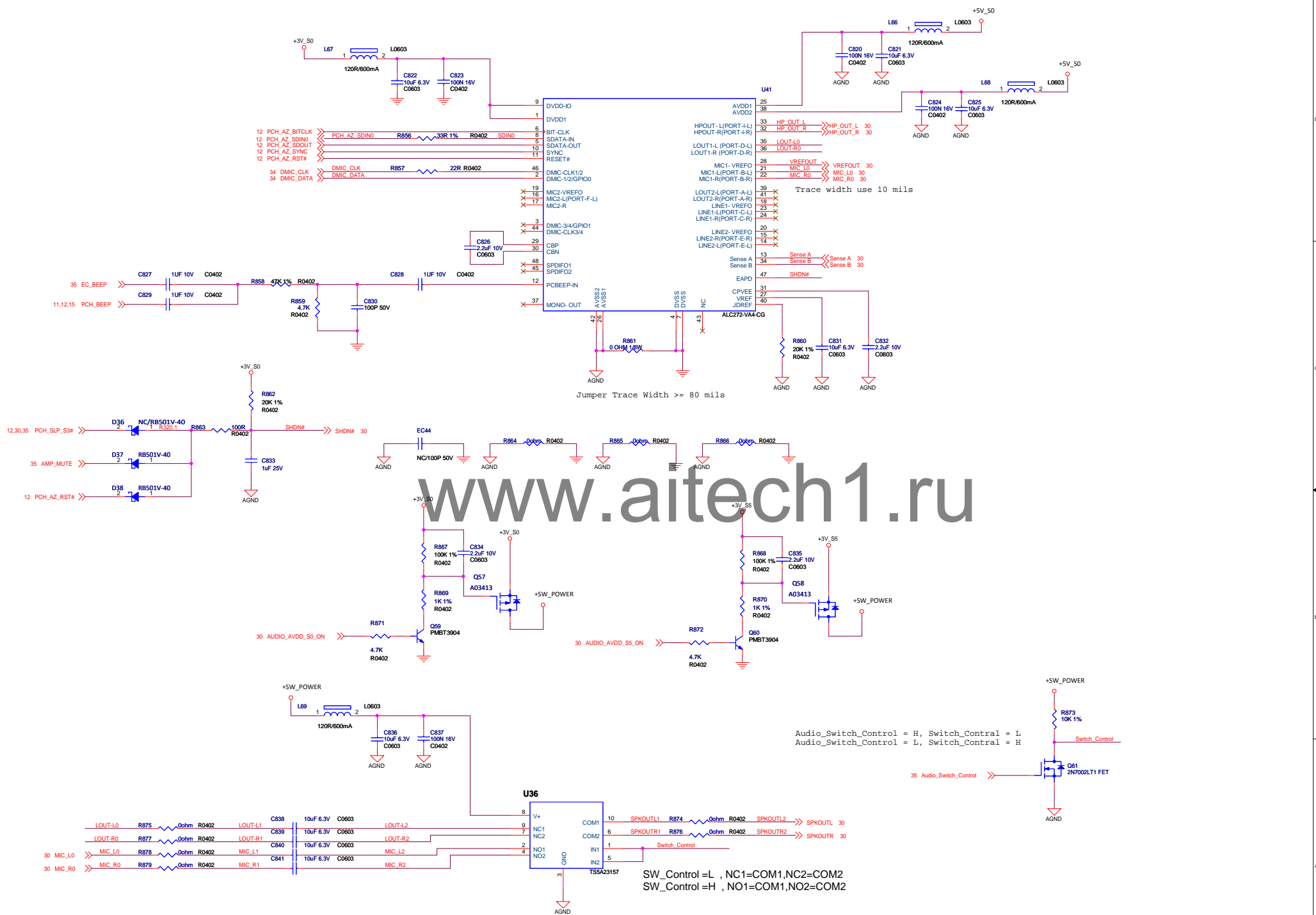


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2		Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina		Rev	ROA
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXXXXXX			
Date	Thursday, December 22, 2011	Sheet	27 of 40		remark	<remark>

LENOVO PIN DEF.



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2		Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina		Rev	RDA
Key Component	Cover SHEET	PCB NAME	XXXXXXXXXXXXXX		remark	<remark>
Date	Thursday, December 22, 2011	Sheet	28 of 49			

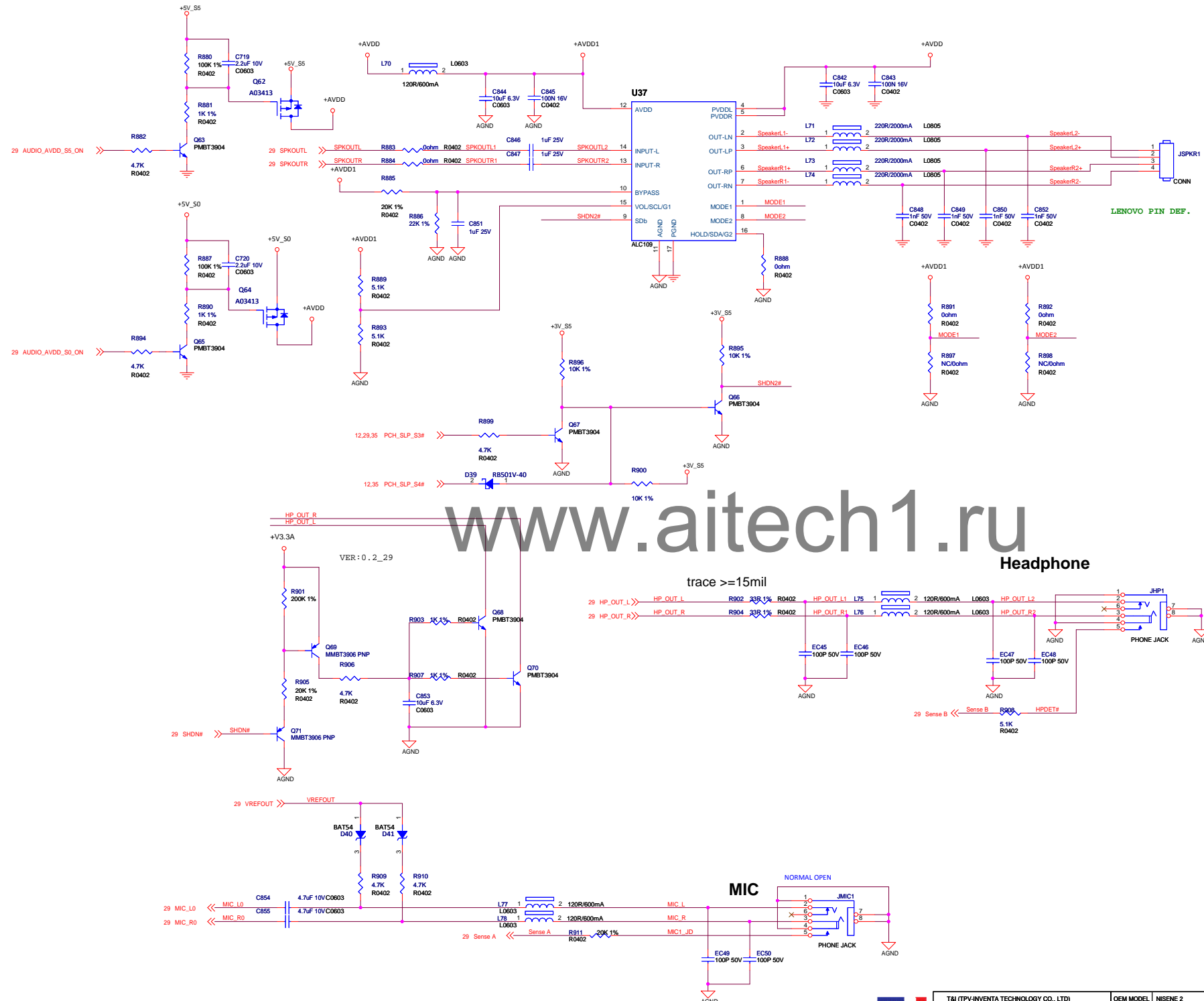


Audio\_Switch\_Control = H, Switch\_Contral = L  
Audio\_Switch\_Control = L, Switch\_Contral = H

SW\_Control=L , NC1=COM1,NC2=COM2  
SW\_Control=H , NO1=COM1,NO2=COM2



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	Rev
Date	Thursday, December 22, 2011	Sheet	29 of 49	remark



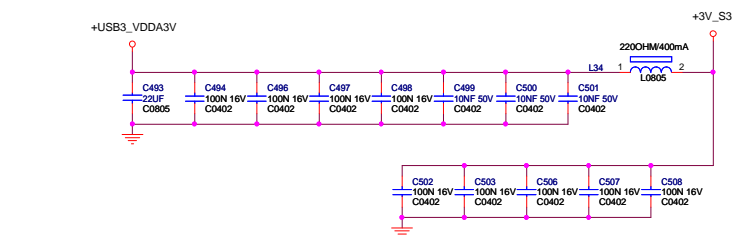
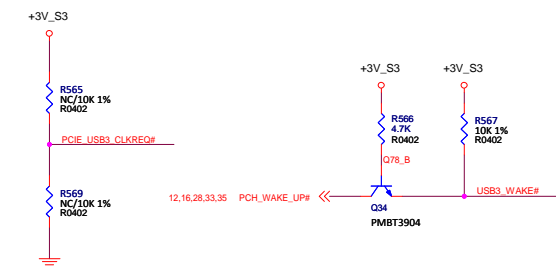
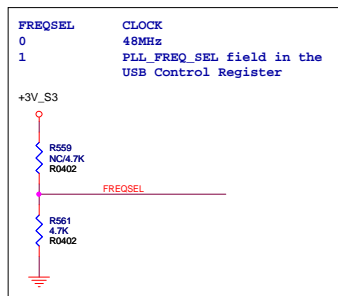
www.aitech1.ru

Headphone

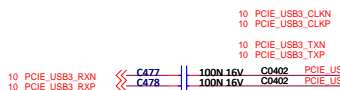
trace >=15mil



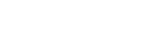
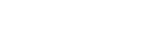
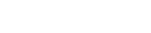
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark
Date	Thursday, December 22, 2011	Sheet	30 of 49	<remarks>



POPULATE PULLDOWN IF I2C EEPROM  
NOT USED AND DO NOT POPULATE  
PULLUP.



PLACE CLOSE TO U1



R1091 FOR WAKE SUPPORT



R1092 FOR NO WAKE SUPPORT



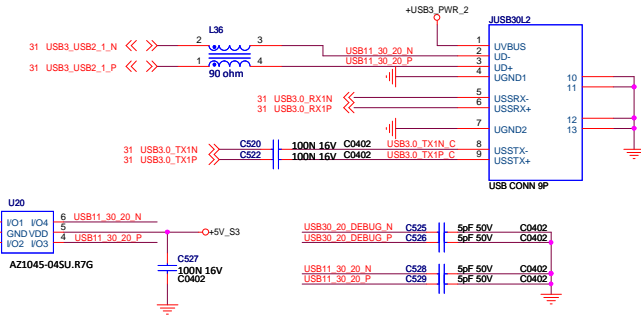
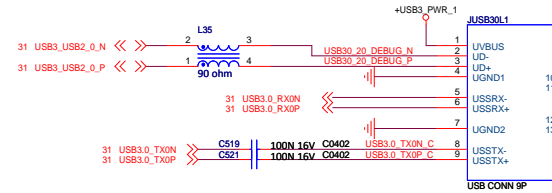
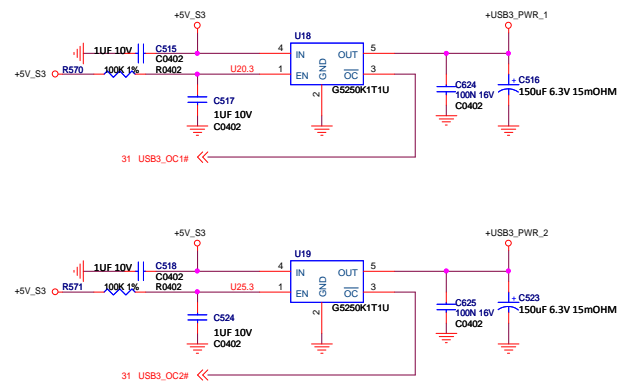
TUSB7320

www.aitech1.ru



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Thursday, December 22, 2011	Sheet	31 of 49	<remarks>

## USB 3.0 (Side IO)



[www.aitech1.ru](http://www.aitech1.ru)

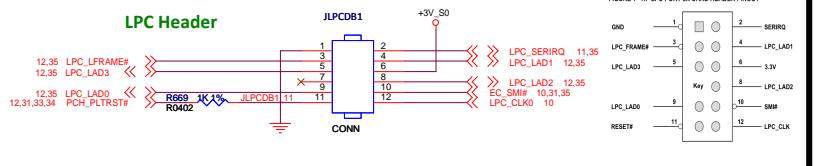




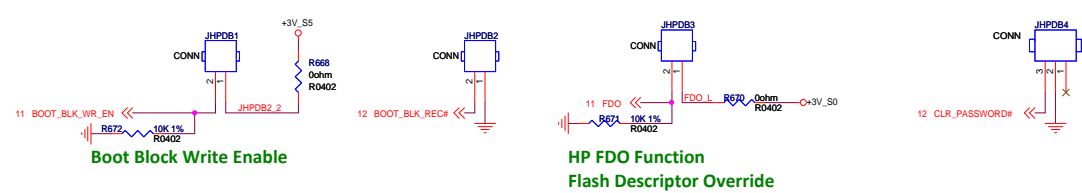




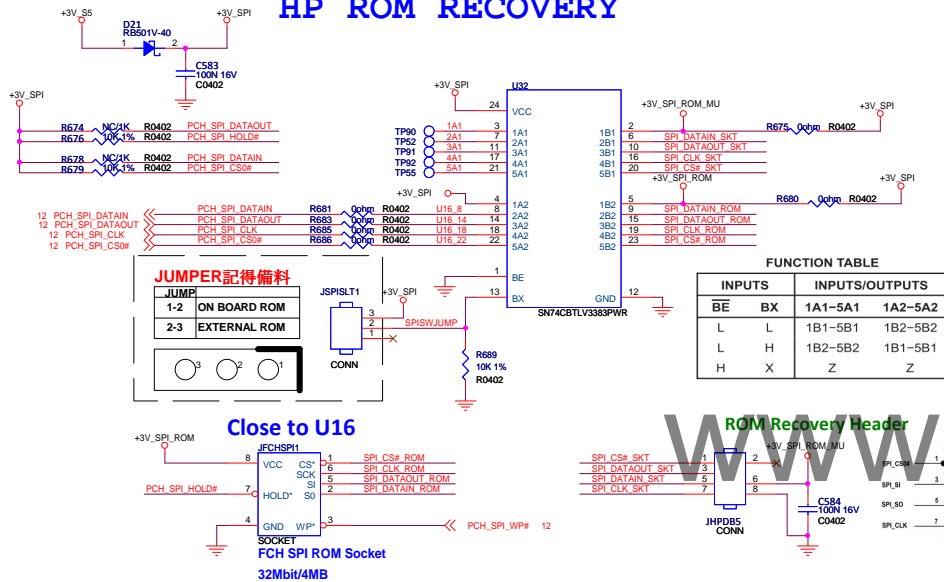
## HP LPC DEBUG PIN HEADER



## HP REQUEST PIN HEADER

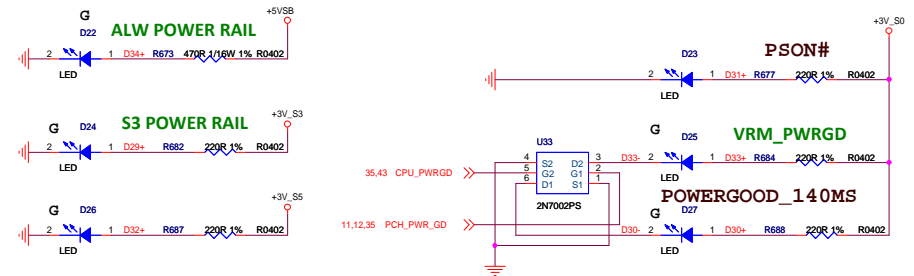


## HP ROM RECOVERY



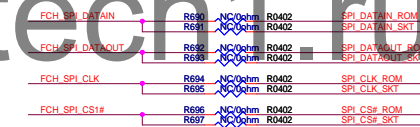
## AUX\_POWER

## HP Indicator LED

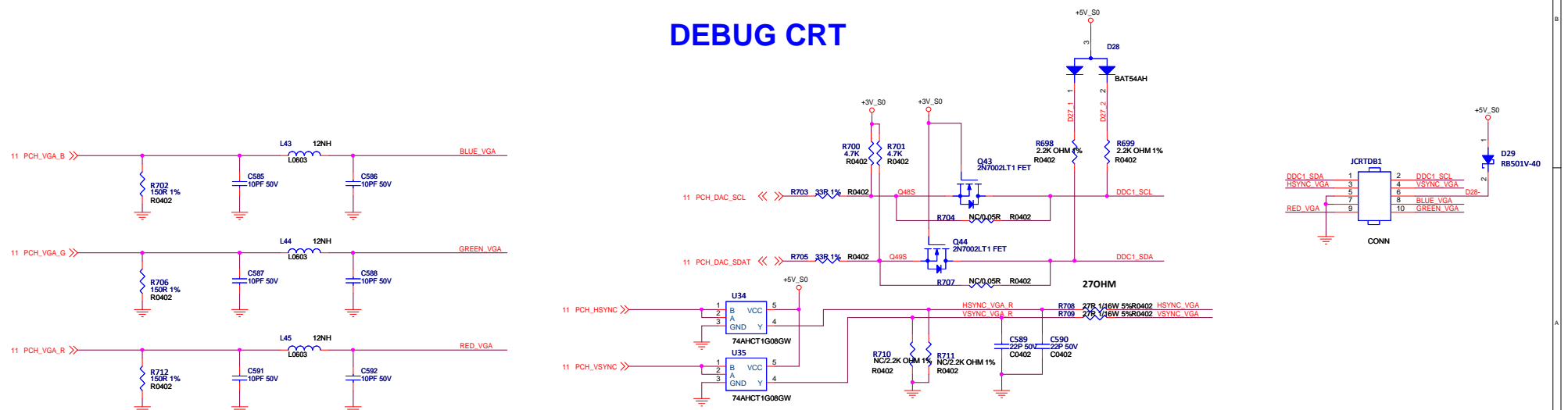


### Close to U16

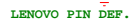
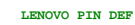
### ROM Recovery Header



## DEBUG CRT

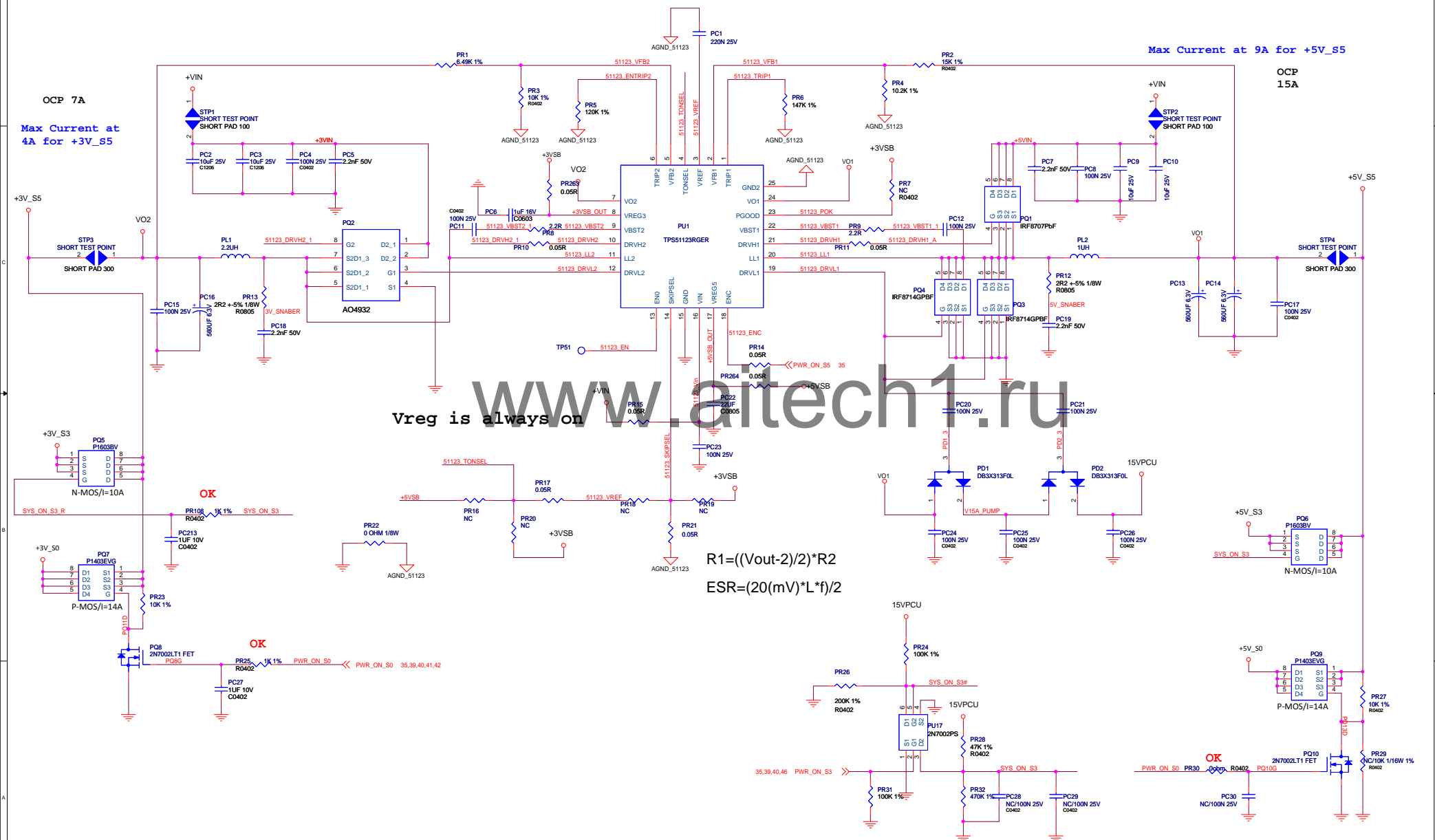


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NIENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev
COVER SHEET	PCB NAME	X00000000000	remark	<remarks>
Date	Thursday, December 22, 2011	Sheet	36 of 48	1

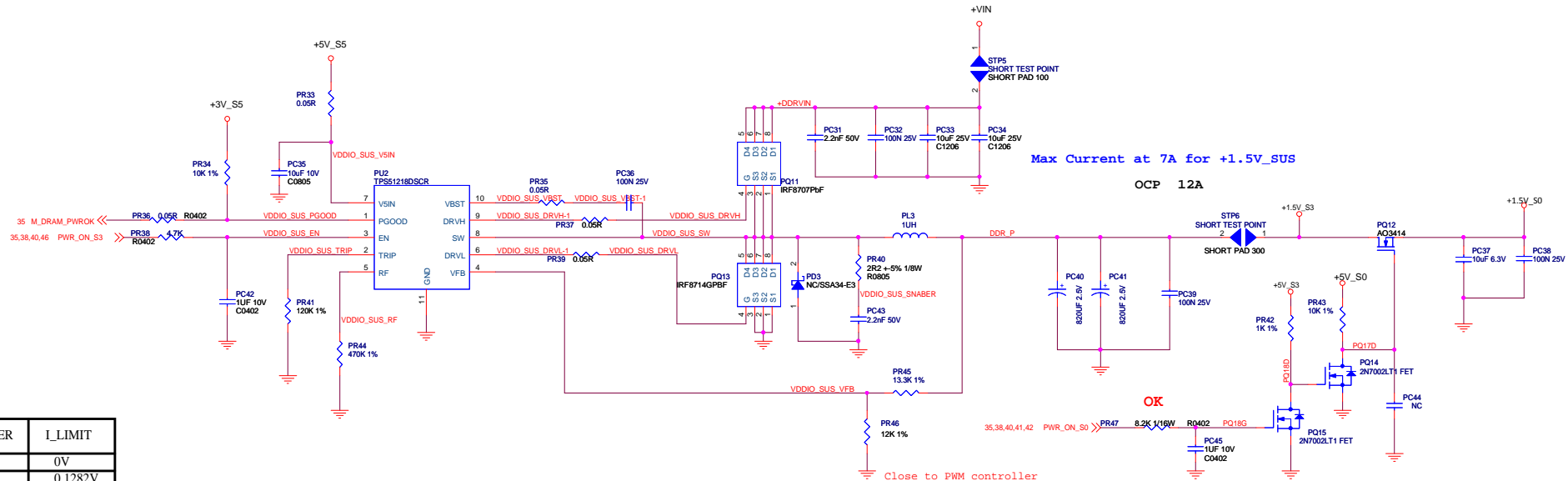


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev	R0A
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark	<remark>
Date	Thursday, December 22, 2011	Sheet	37 of 49		

**SYSTEM +3V\_S5/+3V\_S3/+3V\_S0  
+5V\_S5/+5V\_S3/+5V\_S0**



# +1.5V\_SUS, MEM\_VTT, DC-IN

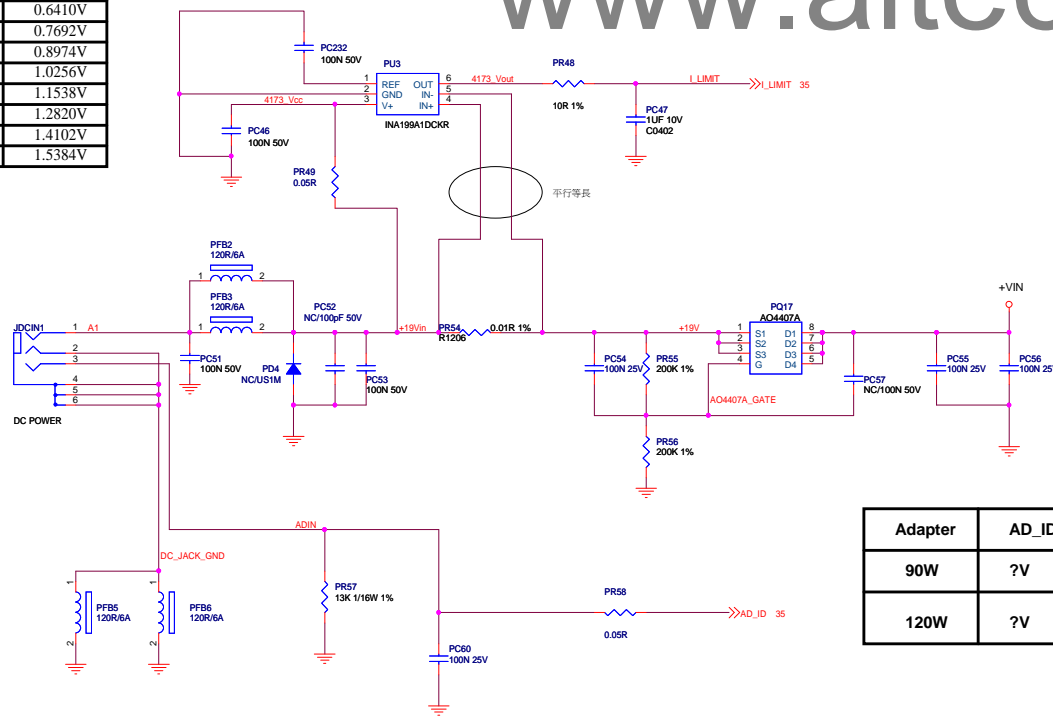


TOTAL POWER	I_LIMIT
0W	0V
10W	0.1282V
20W	0.2564V
30W	0.3846V
40W	0.5128V
50W	0.6410V
60W	0.7692V
70W	0.8974V
80W	1.0256V
90W	1.1538V
100W	1.2820V
110W	1.4102V
120W	1.5384V

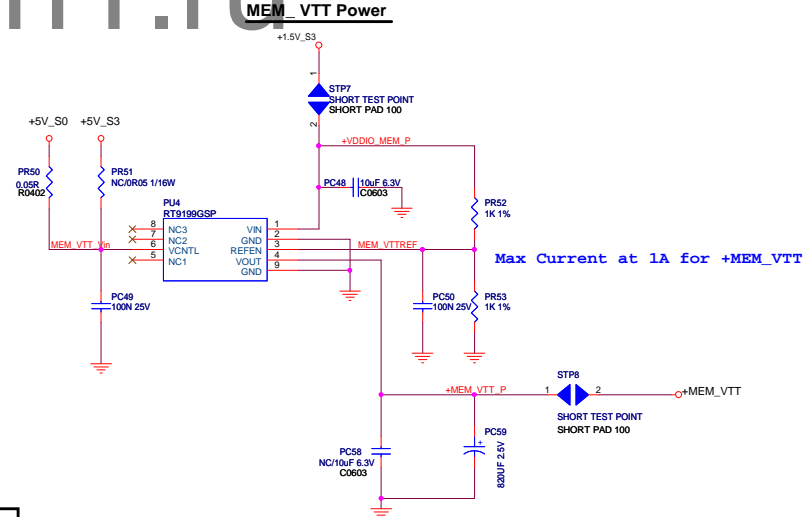
$$V_{out} = 0.704V * (R1 + R2) / R2$$

$$ESR = L * f / 70$$

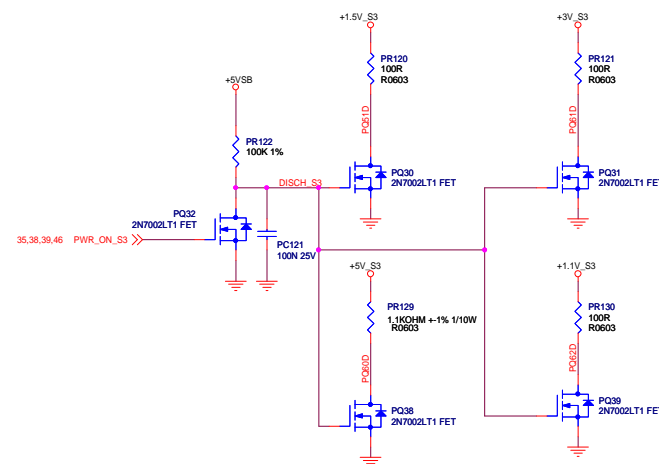
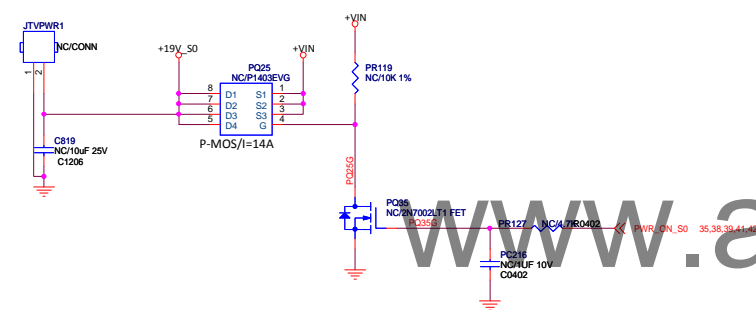
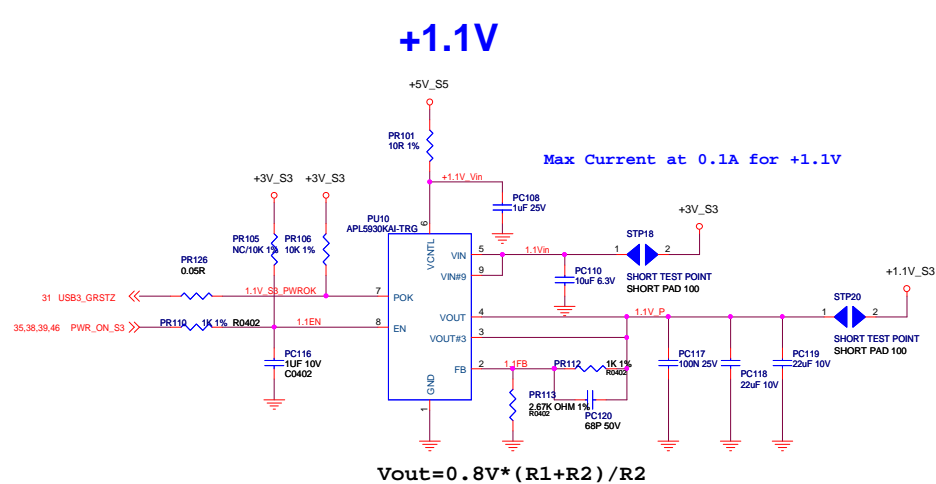
www.aitech1.ru



Adapter	AD_ID
90W	?V
120W	?V



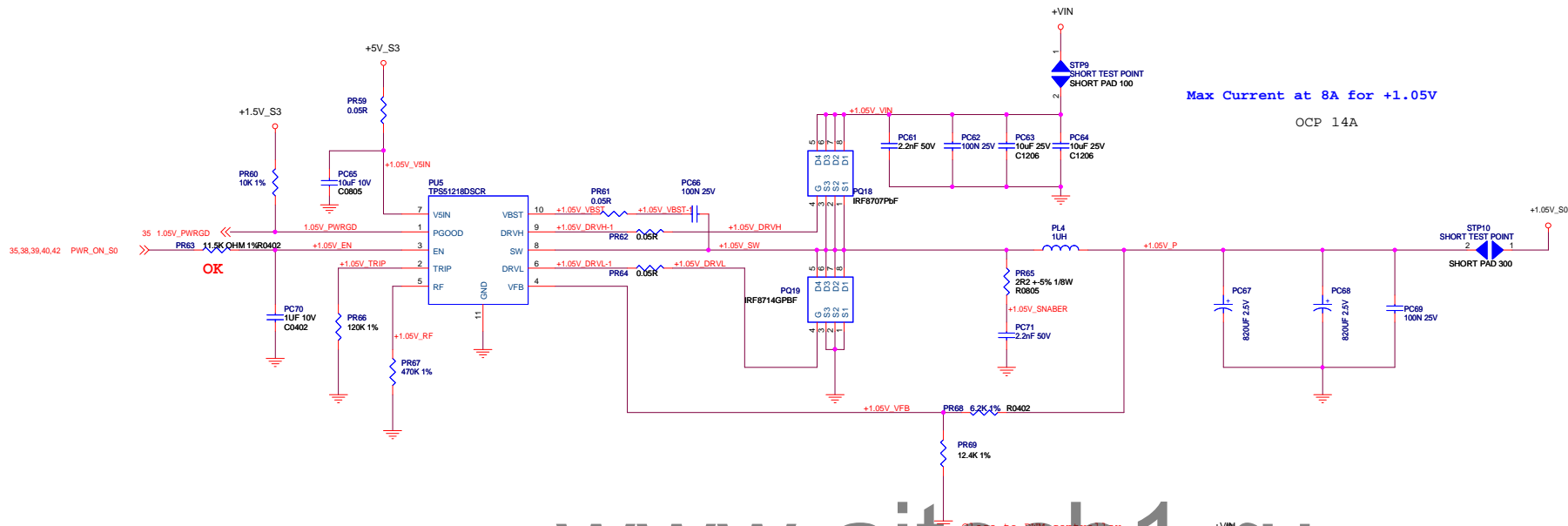
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	COVER SHEET	T&I MODEL	Argentina	Rev
Key Component	PCB NAME	X00000000000000000000	remark	remark
Date	Thursday, December 22, 2011	Sheet	39 of 49	



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2		Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina		Rev	RDA
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX			
Date	Thursday, December 22, 2011	Sheet	40 of 49		remark	<remark>

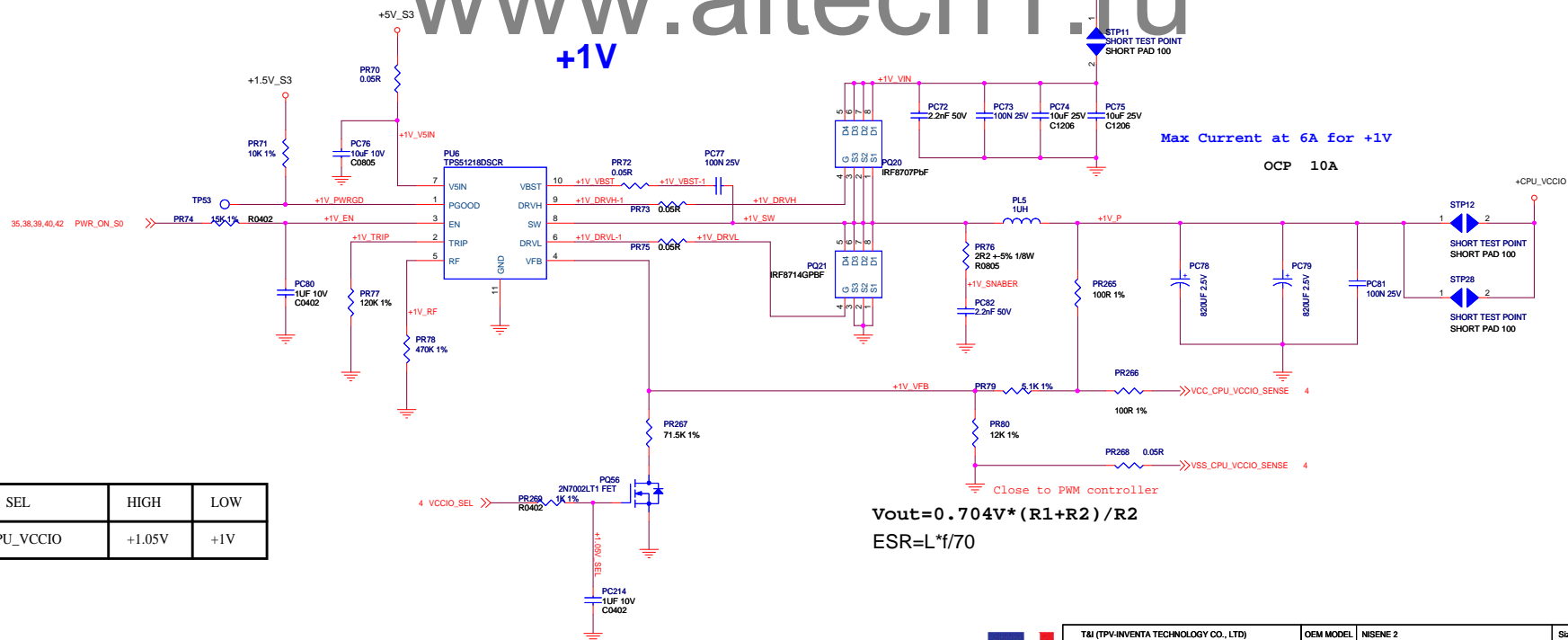


+1.05V



www.aitech1.ru

+1V



SEL	HIGH	LOW
+CPU_VCCIO	+1.05V	+1V

$$V_{out} = 0.704V * (R1 + R2) / R2$$

$$ESR = L * f / 70$$



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev
COVER SHEET		PCB NAME	XXXXXXXXXXXXX	RBA
Key Component		Sheet	41 of 49	remark
Date	Thursday, December 22, 2011			<remarks>

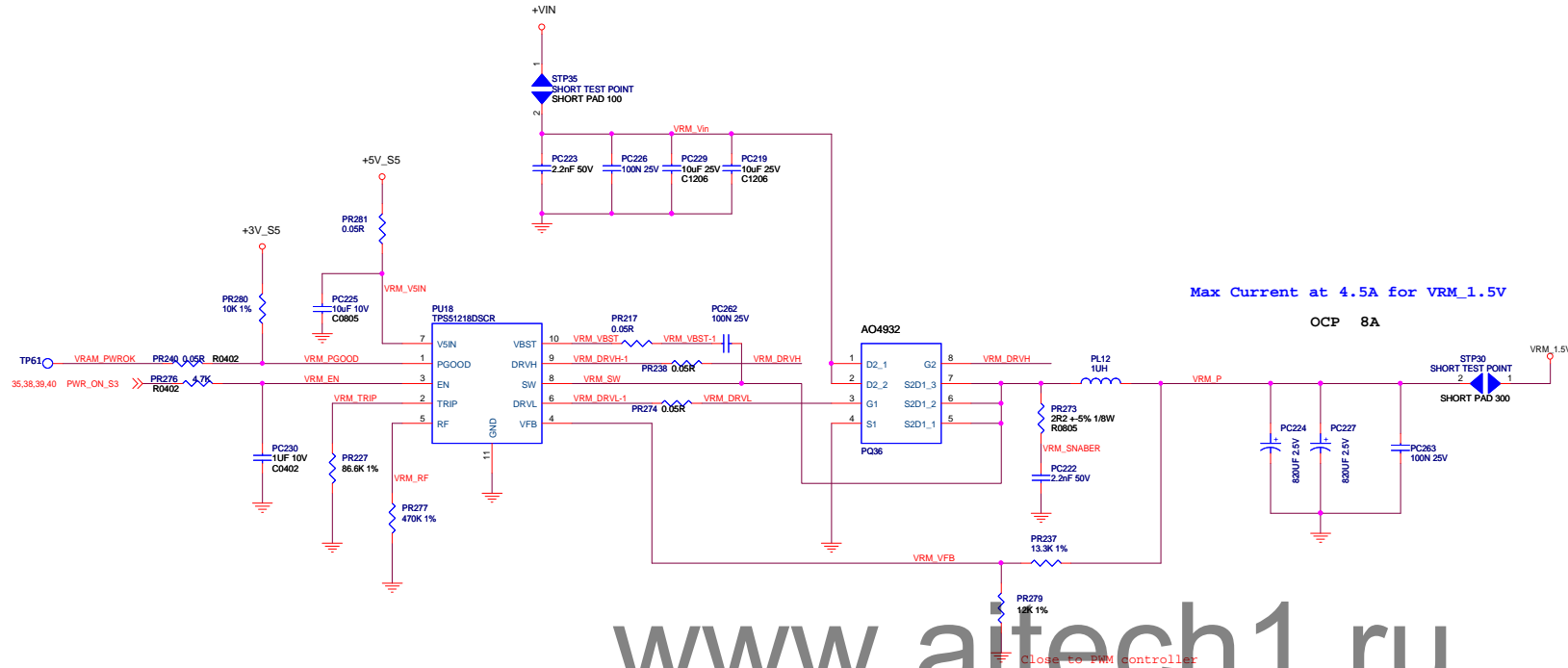








# VRAM\_1.5V



Max Current at 4.5A for VRM\_1.5V

OCP 8A

www.aitech1.ru

$$V_{out} = 0.704V * (R1 + R2) / R2$$

$$ESR = L * f / 70$$

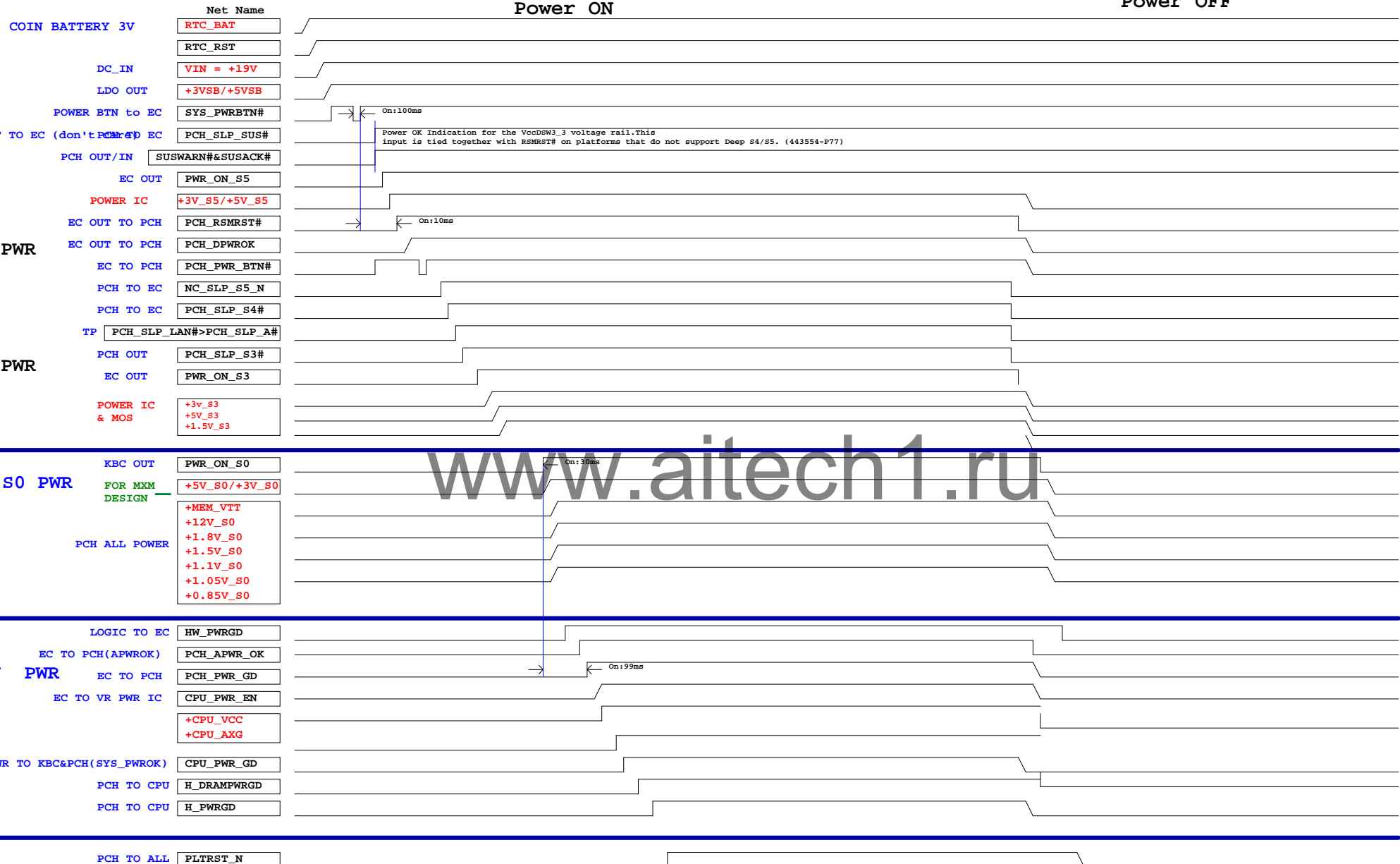


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXX	Rev
Date	Thursday, December 22, 2011	Sheet	46 of 49	remark

# POWER SEQUENCE

Power ON

Power OFF



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXX	RBA
Date	Thursday, December 22, 2011	Sheet	47 of 48	remark
				<remark>

Hudson Fusion Controller HubGPIO Table											
PIN NAME	PIN#	POWER WELL	USAGE	Default Type	Default Value	During Reset	S1	S3	S4/S5	Enable Setting	Note
GPIO0	A3	MAIN	NC	AD0	Output	HIGH					
GPIO1	A5	MAIN	PDO	AD1	Output	HIGH					
GPIO2	A04	MAIN	NC	AD2	Output	HIGH					
GPIO3	A07	MAIN	NC	AD3	Output	HIGH					
GPIO4	A03	MAIN	NC	AD4	Output	HIGH					
GPIO5	A5	MAIN	NC	AD5	Output	HIGH					
GPIO6	A1	MAIN	NC	AD6	Output	HIGH					
GPIO7	A05	MAIN	NC	AD7	Output	HIGH					
GPIO8	A06	MAIN	NC	AD8	Output	HIGH					
GPIO9	A1	MAIN	NC	AD9	Output	HIGH					
GPIO10	A08	MAIN	NC	AD10	Output	HIGH					
GPIO11	A3	MAIN	NC	AD11	Output	HIGH					
GPIO12	A07	MAIN	NC	AD12	Output	HIGH					
GPIO13	A06	MAIN	NC	AD13	Output	HIGH					
GPIO14	A08	MAIN	NC	AD14	Output	HIGH					
GPIO15	A08	MAIN	NC	AD15	Output	HIGH					
GPIO16	A09	MAIN	NC	AD16	Output	HIGH					
GPIO17	A01	MAIN	NC	AD17	Output	HIGH					
GPIO18	A10	MAIN	NC	GP18	Output	HIGH					
GPIO19	A12	MAIN	NC	GP19	Output	HIGH					
GPIO20	A03	MAIN	NC	AD20	Output	HIGH					
GPIO21	A02	MAIN	NC	AD21	Output	HIGH					
GPIO22	A02	MAIN	MMIO_PSSWRT#	AD22	Output	HIGH					
GPIO23	A02	MAIN	PCI_AD23	AD23	Output	HIGH					
GPIO24	AC12	MAIN	PCI_AD24	AD24	Output	HIGH					
GPIO25	A03	MAIN	PCI_AD25	AD25	Output	HIGH					
GPIO26	A03	MAIN	PCI_AD26	AD26	Output	HIGH					
GPIO27	A03	MAIN	PCI_AD27	AD27	Output	HIGH					
GPIO28	A04	MAIN	NC	AD28	Output	HIGH					
GPIO29	A05	MAIN	NC	AD29	Output	HIGH					
GPIO30	AC15	MAIN	NC	AD30	Output	HIGH					
GPIO31	AE16	MAIN	PCB_AD31	AD31	Output	HIGH					
GPIO32	AF18	MAIN	NC	INTF8	HIGH						Internal PU 8.2K
GPIO33	AF19	MAIN	NC	INTF9	HIGH						Internal PU 8.2K
GPIO34	AC16	MAIN	NC	INTF0	HIGH						Internal PU 8.2K
GPIO35	A08	MAIN	NC	INTF0	HIGH						Internal PU 8.2K
GPIO36	AF1	MAIN	PCI_CLK1	PC1CLK	CLK						Output 33MHz
GPIO37	AF5	MAIN	Test Point	PC1CLK	CLK						Output 33MHz
GPIO38	A02	MAIN	PCI_CLK3	PC1CLK	CLK						Output 33MHz
GPIO39	AF6	MAIN	PCI_CLK4	PC1CLK	CLK						14M_OSC/Output 33MHz
GPIO40	A03	MAIN	REQ0	REQ0	HIGH						Internal PU 15K
GPIO41	AF15	MAIN	REQ28	REQ28	HIGH						Internal PU 15K
GPIO42	AM17	MAIN	REQ18	GP1	HIGH						Internal PU 15K
GPIO43	A026	MAIN	PCB_SCL0_Q	GP1	Tri-State						
GPIO44	AD17	MAIN	GNF18	REQ28	Output/HIGH						
GPIO45	AD21	MAIN	GNF28	REQ28	Output/HIGH						
GPIO46	AE17	MAIN	GNF18	GP1	HIGH						Internal PU 8.2K
GPIO47	AD25	MAIN	PCB_SDA0_Q	GP1	Tri-State						
GPIO48	A19	MAIN	LPC_SERIALQ	GP1	HIGH						Internal PU 8.2K
GPIO49	AE27	MAIN	LPC_SERIALQ	GP1	HIGH						Internal PU 8.2K
GPIO50	AE26	MAIN	MMIO_PWB_GOOD	GP1	HIGH						Internal PU 8.2K
GPIO51	A026	MAIN	NC	GP1	HIGH						Internal PU 8.2K
GPIO52	A016	MAIN	Test Point	GP1	HIGH						Internal PU 8.2K
GPIO53	AM15	MAIN	Test Point	GP1	HIGH						Internal PU 8.2K
GPIO54	A16	MAIN	Test Point	GP1	HIGH						Internal PU 8.2K
GPIO55	AM17	MAIN	NC	GP1	HIGH						Internal PU 8.2K
GPIO56	AE15	MAIN	Test Point	GP1	HIGH						Internal PU 8.2K
GPIO57	AM16	MAIN	Test Point	GP1	HIGH						Internal PU 8.2K
GPIO58	AE16	MAIN	Test Point	GP1	HIGH						Internal PU 8.2K
GPIO59	AE18	MAIN	NC	GP1	HIGH						Internal PU 8.2K
GPIO60	AF22	MAIN	PCB_PROGBOOT	GP1	HIGH						Internal PU 8.2K
GPIO61	A022	MAIN	PC1E_PU_CLKREQ0	GP1	HIGH						Internal PU 8.2K
GPIO62	A025	MAIN	PC1E_LAN_CLKREQ0	GP1	HIGH						Internal PU 8.2K
GPIO63	AE24	MAIN	PC1E_WLAN_CLKREQ0	GP1	HIGH						Internal PU 8.2K
GPIO64	A024	MAIN	MMIO_CLK_REQ0	GP1	HIGH						Internal PU 8.2K
GPIO65	AF25	MAIN	PCB_IDLEEXIT#	GP1	HIGH						Internal PU 8.2K
GPIO66	AF28	MAIN	PCB_BUSY	GP1	Tri-State						
GPIO67	AD22	MAIN	SATA_LED#	GP1(OD)	Tri-State						
GPIO68	M28	MAIN	PCB_HSYNC	VDA_HSYNC	Output LOW						
GPIO69	M30	MAIN	PCB_HSYNC	VDA_HSYNC	Output LOW						
GPIO70	M33	MAIN	PCB_DMC_S0AT	VDA_DDC_S0A	Tri-State						
GPIO71	M32	MAIN	PCB_DMC_SCL	VDA_DDC_SCL	Tri-State						
GPIO73	AM14	MAIN	Test Point	GP1	HIGH						Internal PU 8.2K
GPIO74	AM14	MAIN	Test Point	GP1	HIGH						Internal PU 8.2K
GPIO75	A112	MAIN	Test Point	GP1	HIGH						Internal PU 8.2K
GPIO76	AM12	MAIN	Test Point	GP1	HIGH						Internal PU 8.2K
GPIO77	AE13	MAIN	Test Point	GP1	HIGH						Internal PU 8.2K
GPIO78	AM13	MAIN	Test Point	GP1	HIGH						Internal PU 8.2K
GPIO79	AM15	MAIN	Test Point	GP1	HIGH						Internal PU 8.2K
GPIO80	A114	MAIN	Test Point	GP1	HIGH						Internal PU 8.2K

Hudson Fusion Controller HubGPIO Table											
PIN NAME	PIN#	POWER WELL	USAGE	Default Type	Default Value	During Reset	S0	S3	S4/S5	Enable Setting	Note
GPIO111	V1	RESUME	PCB_SPI_WF#	LOW_PST#	Output LOW						
GPIO182	V3	RESUME	PCB_SPI_CLK	SPI_CLK	LOW						Internal PU 10K
GPIO183	V5	RESUME	PCB_SPI_DATAOUT	SPI_DO	LOW						Internal PU 10K
GPIO184	V6	RESUME	PCB_SPI_DATAIN	SPI_DI	LOW						Internal PU 10K
GPIO185	V6	RESUME	PCB_SPI_CS1#	SPI_CS1#	HIGH						Internal PU 10K
GPIO186	V21	RESUME	Test Point	SPI_CS2#	HIGH						Internal PU 10K
GPIO187	A02	RESUME	PCB_AS_SDIO0	AS_SDIO3	LOW						Internal PU 50K
GPIO188	V5	RESUME	Test Point	AS_SDIO2	LOW						Internal PU 50K
GPIO189	V3	RESUME	Test Point	AS_SDIO1	LOW						Internal PU 50K
GPIO190	V1	RESUME	Test Point	AS_SDIO0	LOW						Internal PU 50K
GPIO191	K6	RESUME	PD_10K	GP1							
GPIO192	K5	RESUME	PD_10K	GP1							
GPIO193	K3	RESUME	PD_10K	GP1							
GPIO194	M6	RESUME	APU_ALARM#	GP1							Internal PU/PD(disable by default) 10K
GPIO195	M2	RESUME	APU_P0_WAKE#	GP1							Internal PU/PD(disable by default) 10K
GPIO196	M3	RESUME	PCB_VIN1	GP1							Internal PU/PD(disable by default) 10K
GPIO197	L2	RESUME	PCB_VIN2	GP1							Internal PU/PD(disable by default) 10K
GPIO198	M1	RESUME	PCB_VIN3	GP1							Internal PU/PD(disable by default) 10K
GPIO199	P1	RESUME	PCB_VIN4	GP1							Internal PU/PD(disable by default) 10K
GPIO180	P3	RESUME	PCB_VIN5	GP1							Internal PU/PD(disable by default) 10K
GPIO181	M1	RESUME	PCB_VIN6	GP1							Internal PU/PD(disable by default) 10K
GPIO182	M5	RESUME	PCB_VIN7	GP1							
GPIO183	M8	RESUME	Test Point	GP1							Internal PU 10K
GPIO184	V2	RESUME	NC	GP1							Internal PU 10K
GPIO185	M6	RESUME	Test Point	USB_PSDOP	LOW						Internal PU 15K
GPIO186	M1	RESUME	Test Point	USB_PSDIP	LOW						Internal PU 15K
GPIO187	K13	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO188	J19	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO189	D21	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO190	C20	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO191	D23	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO192	C22	RESUME	Test Point	GP1	HIGH						
GPIO193	B19	RESUME	PCB_SCL0	GP1	Tri-State						
GPIO194	B19	RESUME	PCB_SDA2	GP1	Tri-State						
GPIO195	D22	RESUME	PCB_SCL3	GP1	Tri-State						
GPIO196	D21	RESUME	PCB_SDA1	GP1	Tri-State						Internal PU 10K
GPIO197	E22	RESUME	NC	GP1	HIGH						Internal PU 10K
GPIO198	E22	RESUME	NC	GP1	HIGH						Internal PU 10K
GPIO199	V22	RESUME	PCB_GP10199	GP1	HIGH						Internal PU 10K
GPIO200	B21	RESUME	NC	GP1	HIGH						Internal PU 10K
GPIO201	E21	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO202	E22	RESUME	CLR_PASSWORD_L	GP1	HIGH						Internal PU 10K
GPIO203	F22	RESUME	BOOT_BLK_WF_EN_R	GP1	HIGH						Internal PU 10K
GPIO204	E24	RESUME	BOOT_BLK_WF_EN_L	GP1	HIGH						Internal PU 10K
GPIO205	E24	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO206	B23	RESUME	CLR_BIOS_DATA_L	GP1	HIGH						Internal PU 10K
GPIO207	C24	RESUME	NC	GP1	HIGH						Internal PU 10K
GPIO208	F18	RESUME	NC	GP1	HIGH						Internal PU 10K
GPIO209	F21	RESUME	PCB_MB_ID0	GP1	HIGH						Internal PU 10K
GPIO210	E20	RESUME	PCB_MB_ID1	GP1	HIGH						Internal PU 10K
GPIO211	F20	RESUME	PCB_MB_ID2	GP1	HIGH						Internal PU 10K
GPIO212	A22	RESUME	PCB_MB_ID3	GP1	HIGH						Internal PU 10K
GPIO213	F18	RESUME	PCB_MB_ID4	GP1	HIGH						Internal PU 10K
GPIO214	A20	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO215	J18	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO216	B18	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO217	G18	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO218	B21	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO219	F16	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO220	D19	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO221	A18	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO222	C18	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO223	B19	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO224	B17	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO225	A18	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO226	D17	RESUME	Test Point	GP1	HIGH						Internal PU 10K
GPIO227	F7	RESUME	PCB_SCL1_Q	GP1	Tri-State						
GPIO228	F7	RESUME	PCB_SCL1_Q	GP1	Tri-State						
GPIO229	C24	RESUME	DP_VDDP_R	DP_VDDP	Output/HIGH						

www.aitech1.ru



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2		Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Argentina		Rev	RDA
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX		remark	<remark>
Date	Thursday, December 22, 2011	Sheet	48 of 48			



Schematic Modify History

PVT & MP de-pop circuit

page 16 for EC debug connector  
JECDB1

page 17 for HP debug  
JLPCDB1,R310,JHPDB5,C147,U31,Q22,D9~D14,R312~R317

page 17 for AMD debug  
U5,R53,R56,R77,R80

page 17 for TnI HW debug (CRT output function)  
C3,C4,C7,C14,C15,C16,C21,C22,D22,D23,JCRTDB1  
L1,L2,L3,Q1,Q2,R1,R2,R3,R4,R5,R6,R10,R11,R14  
R15,R25,R26,R28,R29,R30,R32,R36,R37,U1,U2

www.aitech1.ru



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2		Size	C
Circuit diagram NO.		<Circuit diagram NO.>		T&I MODEL	Argentina	Rev RBA
Key Component		COVER SHEET		PCB NAME	XXXXXXXXXXXX	
Date		Thursday, December 22, 2011		Sheet	49 of 49	remark <remark>